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RAYTHEON COMPANY
EQUIPMENT DIVISION

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TABLE OF CONTENTS

<u>SECTION</u>	<u>PAGE</u>
1. INTRODUCTION	1-1
1.1 Overall Arrangement	1-1
1.2 Performance Description	1-1
1.3 Spectrum Analyzer	1-4
2. PHYSICAL DESIGN	2-1
3. INPUT/OUTPUT INTERFACES	3-1
3.1 Signal Inputs from Laser-Optics Assembly	3-1
3.1.1 With Translator	3-1
3.1.2 Without Translator	3-2
3.2 Binary Interconnections with Scanner	3-2
3.3 Digital Recorder Interconnections	3-2
3.4 Display Interconnections	3-3
3.5 Analog Recorder Interconnections	3-3
3.6 Remote Control Interconnections	3-3
4. PERFORMANCE CHARACTERISTICS	4-1
4.1 Velocity Coverage Resolution	4-1
4.2 Signal Integration	4-1
5. SUB-ASSEMBLY DESIGN	5-1
5.1 Spectrum Analyzer	5-1
5.1.1 Introduction	5-1
5.1.2 RF Section	5-1
5.1.3 Impulse Generator	5-6
5.1.4 Weighting Circuit	5-6
5.1.5 Gain Control Circuit	5-7
5.2 Spectrum Integrator	5-10
5.2.1 A/D Converter Card	5-11
5.2.2 Accumulator Card	5-15
5.2.3 Output Card	5-17
5.3 Velocity Discriminator	5-21
5.4 Display Interface	5-23
5.4.1 Function	5-23
5.4.2 Modes	5-23
5.4.3 Display Buffer Card	5-24
5.4.4 Display Driver Card	5-30
5.4.5 Analog Recording	5-33
5.5 Formatter	5-33
6. OPERATIONAL CHECKS	6-1
6.1 Power On	6-1
6.2 Spectrum Analyzer	6-1
6.3 Signal Integration and Velocity Discrimination	6-2
6.4 Display	6-2
6.5 Formatter Frame Counter	6-3
7. PERFORMANCE TESTS	7-1
7.1 Velocity Coverage	7-1
7.1.1 Test Description	7-1
7.1.2 Test Procedure	7-2

TABLE OF CONTENTS continued

SECTION	PAGE
7.2 Velocity Resolution	7-2
7.2.1 Test Description	7-2
7.2.2 Test Procedure	7-3
7.3 Dynamic Range	7-3
7.3.1 Test Description	7-3
7.3.2 Test Procedure	7-3
7.4 CFAR Mode	7-4
7.4.1 Test Description	7-4
7.4.2 Test Procedure	7-4
7.5 A/D Conversion	7-5
7.5.1 Test Description	7-5
7.5.2 Test Equipment Required	7-5
7.5.3 Test Procedure	7-6
7.6 Integration Time	7-7
7.6.1 Test Description	7-7
7.6.2 Equipment Required	7-7
7.6.3 Test Procedure	7-8
7.7 Width Integration (Velocity Discriminator)	7-9
7.7.1 Test Description	7-9
7.7.2 Test Procedure	7-9
7.8 Velocity Threshold (Velocity Discriminator)	7-10
7.8.1 Test Description	7-10
7.8.2 Test Procedure	7-11
7.9 Amplitude Threshold (Velocity Discriminator)	7-11
7.9.1 Test Description	7-11
7.9.2 Test Procedure	7-12
7.10 Density Mode (Velocity Discriminator)	7-13
7.10.1 Test Description	7-13
7.10.2 Test Procedure	7-13
7.11 Display Interface	7-14
7.11.1 Test Description	7-14
7.11.2 Test Procedure	7-14
7.12 Scanner Interface	7-16
7.12.1 Test Description	7-16
7.12.2 Test Procedure	7-16
7.13 Analog Recorder Interface	7-16
7.13.1 Recording	7-16
7.13.2 Playback	7-17
7.14 Formatter	7-17
7.14.1 Test Description	7-17
7.14.2 Test Equipment Required	7-17
7.14.3 Test Procedure	7-17
8. PROCESSOR MODIFICATIONS	8-1
Appendix A Implementation of IF Filter Banks Using Dispersive Delay Lines	A-1
Appendix B PbSnTe Detector Tests	B-1

LIST OF ILLUSTRATIONS

<u>FIGURE</u>		<u>PAGE</u>
1	Overall Block Diagram Signal Processor for Laser Vortex Detection System	1-2
2	Spectrum Analyzer Resolution	4-2
3	Signal Processor Frequency Coverage Chart	4-3
4	Signal Processor Velocity Coverage Chart	4-4
5	Spectrum Analyzer Block Diagram	5-2
6	Spectrum Analyzer RF Section	5-3
7	Impulse Generator Arrangement	5-7
8	Hamming-Weighted Chirp Waveform	5-8
9	Block Diagram of Weighting Function Generation	5-8
9a	Weighting Control Timing Waveforms	5-9
10	Spectrum Integrator Block Diagram	5-12
10a	A/D Converter Waveforms	5-13
10b	Accumulator Waveforms	5-13
11	Integrator Input Timing	5-16
12	Integrator Output Timing	5-19
13	Velocity Discriminator	5-22
14	Display Buffer	5-25
15	Video Control	5-26
16	Vector Generation	5-28
17	Display Resolution	5-31
18	Display Driver	5-32
19	Formatter Block Diagram	5-35
19a	Timing Diagram	5-36
20	Example: Wind Signal Spectrum Analyzer Output	6-4
21	Width Integration and Amplitude Threshold Outputs (Zero)	6-5
22	Width Integration and Amplitude Threshold Outputs (Proper Level)	6-5
23	Integrator Output Converted to Analog	7-8
24	Width Integrator Impulse Response	7-10
25	Velocity Threshold Effect	7-11
26	Amplitude Threshold	7-12
27	Log Converter Characteristic	8-2
28	Log Converter Characteristic	8-3
29	Spectrum Output	8-4

LIST OF TABLES

<u>TABLE</u>		<u>PAGE</u>
I	Signal Processor Front Panel Controls	2-2
II	A/D Conversion Rate Extension	5-14
III	Spectrum Analyzer Cycles-Integration Time	5-18
IV	Scanner Co-ordinates	5-29
V	Output Specifications	5-37
VI	Analog Output Levels	8-5

LIST OF SCHEMATICS AND PARTS BREAKDOWN*

A1	Interconnection Schematic	
A2	Spectrum Analyzer Block Diagram	
A2A1	Input Translator I Schematic Diagram	
A2A2	Input Translator II	" "
A2A3	Frequency Resolver	" "
A2A4	Filter Assembly	" "
A2A5	Limiter	" "
A2A6	Chirp Generator	" "
A2A7	Chirp Translator	" "
A2A8	AGC Circuit	" "
A3	A/D Converter	" "
A3A1	Signal Detector Assembly	" "
A4	Accumulator	" "
A5	Integrator Output	" "
A6	Formatter	" "
A7	Velocity Discriminator	" "
A8	Display Buffer	" "
A9	Display Driver	" "
A10	Weighting Control Generator Schematic Diagram	
A11	+5 Volt Supply	Sorensen STM5-24 Manual
A12	-5 Volt Supply	Powertec 2B5-3 Manual
A13	+15 Volt Supply	Powertec 2L15D-2.8 Manual
A14	+24 Volt Supply	Powertec 2D24-1 Manual
A15	120 Volt DC Power Supply	Schematic Diagram
	Test Card	Schematic Diagram
	Display Driver Parts List	

* Schematics and Parts Lists were previously supplied. This listing represents that which was supplied.

SECTION 1

INTRODUCTION

1.1 OVERALL ARRANGEMENT

A block diagram of the signal processing equipment is given in Figure 1. There are five subdivisions in the overall circuitry provided: (1) the spectrum analyzer, (2) the spectrum integrator, (3) the velocity discriminator, (4) the display interface, and (5) the formatter. They function in series: first in analog form to provide frequency resolution, then in digital form to achieve signal-to-noise improvement (video integration) and frequency discrimination, and finally in analog form again for the purpose of real-time display of the significant velocity data. The formatter collects binary data from various points in the processor and provides a serial output for bi-phase recording.

1.2 PERFORMANCE DESCRIPTION

The signal processor accepts signals from the laser assembly with or without the use of a laser output frequency translator. Overall performance specifications are as follows:

Velocity Coverage Modes

Without translator -	0 to +170 ft/sec
With translator -	0 to <u>+170</u> ft/sec
	-120 to +120 ft/sec
	+100 to +200 ft/sec

Frequency Resolution

Without translator -	150 kHz from 0 to 100 ft/sec
	200 kHz beyond
With translator -	150 kHz from -50 to +50 ft/sec
	200 kHz from <u>+50</u> to <u>+120</u> ft/sec
	150 kHz from +100 to +200 ft/sec

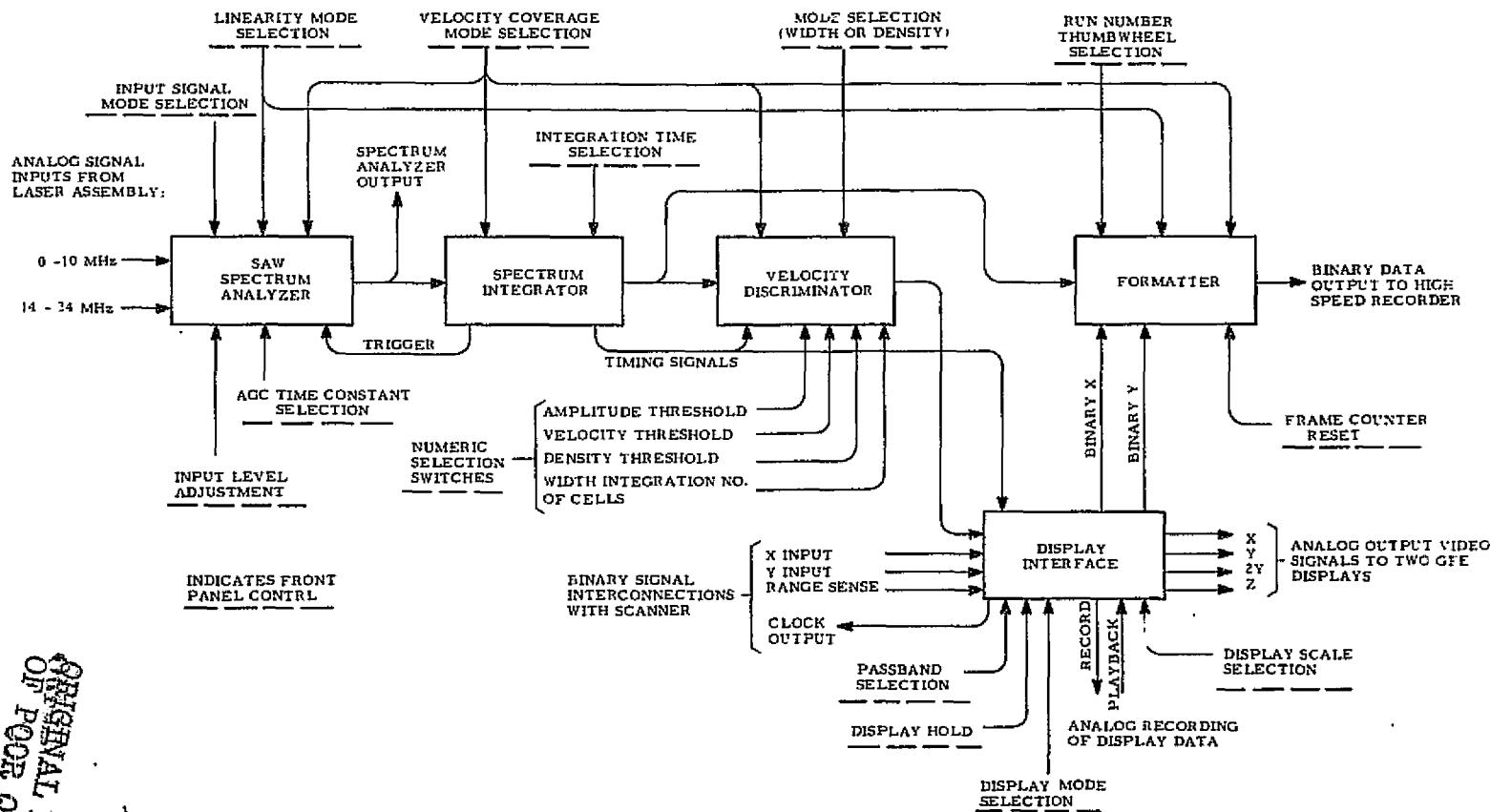


Figure 1 Overall Block Diagram
SIGNAL PROCESSOR FOR LASER VORTEX
DETECTION SYSTEM

Dynamic Range (Output)

Linear mode -	35 dB
CFAR mode -	18 dB
Video Quantification -	8 bit A/D
Integration Time (Video) -	0.5 to 64 msec in selectable binary steps
Velocity Discrimination -	Selectable thresholds for amplitude, minimum velocity, and spectral characteristics.

Display Interface

External input required -	Binary X and Y coordinates from scanner
Output data -	Analog range, altitude, and velocity information display and recording.

The input to the signal processor from the laser assembly is in the frequency range from 0 to 10 MHz for operation without the translator, and in a band centered at 24 MHz for operation with the translator. With the translator, the spectrum analyzer is capable of accepting a band up to 20 MHz wide. The performance of the spectrum analyzer is highest in the center of this band, providing the 100 kHz resolution over a 6 MHz range. Beyond this central range, the resolution and sensitivity decrease depending on the bandpass characteristic of the surface-acoustic-wave (SAW) dispersive delay line used in the spectrum analyzer.

The spectrum integrator performs integration separately on each resolution cell produced by the analyzer. The output for the complete frequency coverage interval is delivered in binary form to the velocity discriminator where thresholds are applied to extract significant information for display. These thresholds are (a) amplitude, to establish the minimum detectable energy level of a spectral component, (b) velocity, to establish the minimum velocity to be accepted, and (c) width or density, to establish the optimum spectral

characteristics of a signal to be detected. The thresholds serve to discriminate against false alarms due to random noise peaks as well as actual signals too low in velocity to be of interest. The false-alarm aspect is particularly important, since the display system could become cluttered with false velocity indications.

Two operating modes are used with respect to the amplitude range of the signals to be processed. For the most efficient detection of a vortex cell, the "CFAR" mode (Constant False-Alarm Rate) is used. This incorporates hard-limiting in the spectrum analyzer and results in the normalizing of the background noise to a constant level in the absence of a true signal. The amplitude threshold can be set for a constant false alarm rate in this case. There is negligible loss in signal-to-noise ratio but there is a modification of the spectral distribution of a signal. To perform a true spectrum analysis of a signal, linear operation must be used. For this, a manual gain adjustment is provided to set the input level within the optimum dynamic range of the processor.

The display interface combines the velocity data from the discriminator with horizontal range and altitude inputs to obtain an analog output suitable for a B-scope display. The display format is designed to be compatible with commercially available display equipment and functions by producing brightening of the display face in areas where the scanned laser beam intercepts velocities above the velocity threshold.

The display interface also has the capability for analog recording of the display information and replay/display.

1.3 SPECTRUM ANALYZER

The spectrum analyzer uses a surface acoustic wave (SAW) delay line technique to provide velocity resolution equivalent to a bank of parallel, narrowband filters. The SAW spectrum analyzer technique is described in the Appendix. "Implementation of 1F Filter Banks Using Dispersive Delay Lines." Briefly, the technique uses two identical delay lines having a

linear frequency-dispersion characteristic. One of the lines is driven repetitively with an impulse, creating a recurring, linear frequency-versus-time scan by means of its dispersion characteristic. This scanning output is frequency-mixed with the input signal to be spectrum analyzed. By inverting the resultant spectrum and passing this through the second delay line, an impulse response is recreated wherein the exact time position of the impulse is a function of the frequency of the input signals. If there is more than one frequency component in the input signal, there will be more than one impulse generated, providing a true spectrum analysis of the signal.

The output of the spectrum analyzer is delivered to the spectrum integrator as a time-ordered, serial set of velocity bins.

SECTION 2

PHYSICAL DESIGN

The overall signal processor, with the exception of the GFE display and hard copy unit, is wholly contained in one unit capable of rack mounting in a standard 19-inch relay-rack. The unit contains all necessary power supplies for operation from 115 volt, 60 hertz primary power.

All input/output signal interconnections are made at the rear of the unit. All controls necessary for the normal operation of the equipment are located on the front panel. Exceptions here are any potentiometer-type adjustments which are used in initially balancing or calibrating levels within the equipment.

Front panel controls are as given in Table I. In addition to these controls, the front panel has two indicator lamps: a green one to indicate the power-on condition, and a red one to indicate a frame counter overflow condition.

The front panel also contains a jack for monitoring the analog signal output of the spectrum analyzer by means of a CRO, plus a jack supplying an appropriate trigger for a CRO.

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TABLE I

SIGNAL PROCESSOR FRONT PANEL CONTROLS

Name of Control	Positions	Function
Velocity Coverage	<ol style="list-style-type: none"> 1. 0 to 100 ft/sec 2. 0 to 170 ft/sec 3. -50 to +50 ft/sec 4. -120 to +120 ft/sec 5. +100 to +200 ft/sec 6. Remote 	Selects velocity coverage mode. Positions 1 and 2 apply to use of the processor either with or without the translator and remaining positions, only with the translator. Positions 1, 3, and 5 are restricted bandwidth, high processor efficiency modes. Position 6 provides for a remote location at which the velocity coverage mode can be selected.
Linearity	<ol style="list-style-type: none"> 1. Linear 2. CFAR 	SPDT toggle to switch limiter in or out in spectrum analyzer.
Input Level	Potentiometer	Manual adjustment of signal level at input to signal processor.
Integration Time	Nine positions	Eight integration time selections (0.5 to 64 msec) plus remoting functions.
Amplitude Threshold	3-digit thumbwheel switch	Decimal selection of one of 200 possible amplitude levels. The level selected applies to both the width integration mode and the density threshold mode.
Velocity Threshold	2-digit thumbwheel switch	Decimal selection of one of 100 possible velocity bins.
Density Threshold	2-digit thumbwheel switch	Decimal selection of one of 20 possible bin multiples.
Velocity Discriminator Mode	Two	Selects either width integration or density mode.

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TABLE I
SIGNAL PROCESSOR FRONT PANEL CONTROLS (Cont)

Name of Control	Positions	Function
Wide Integration Number of Cells	12-position rotary switch	Selects number of contiguous spectrum analyzer cells over which signal is summed.
Run Number	4-digit thumbwheel switch	Decimal selection of one of 10,000 possible numbers.
Frame Counter Reset	Pushbutton	Resets frame counter to zero.
Display Mode	Four	Selects from two different means of displaying velocity information and two different test modes which trace the scanner pattern.
Scale	Three	Provides a choice of three display deflection sensitivities.
Velocity Passband	Three	Provides a means of restricting the displayed velocity data to either the positive or negative doppler sidebands.
Normal/Hold	Two	Prohibits writing new information into the display when in the "hold" position.
Normal/Playback	Two	Determines the source of the displayed data.
AGC Time Constant	1. Short 2. Long	Provides a shorter time constant for use when adjusting the input signal level or AGC threshold.
AGC Threshold	Potentiometer	Determines level at which AGC action begins (delayed AGC).
Input Signal Mode	1. Translated 2. Non-Translated	Determines input signal frequency range for signal processor operation.
Power	Two	Turns on/off self-contained power supplies in signal processor.

SECTION 3

INPUT/OUTPUT INTERFACES

An overall block diagram of the signal processor was given in Figure 1. It will be seen that there are five groups of interconnections between the processor and other parts of the laser vortex system. They are: (1) the interconnections with the laser-optics assembly, (2) interconnections with the scanner, (3) interconnections with a binary data recorder, (4) interconnections with an analog data recorder, (5) interconnections with display units. Additionally, there are connections for remote control selection of the velocity coverage and the integration time. The requirements for each of these is described here.

3.1 SIGNAL INPUTS FROM LASER-OPTICS ASSEMBLY

Two types of analog signals are supplied: (1) a signal arising from use of the optics with the laser translator, and (2) a signal resulting from use without the translator. Only one signal will exist at any time, interconnected to the signal processor by means of either one or two type RG-58 cables terminated with male type BNC connectors. Electrical characteristics of the signals will be as follows.

3.1.1 WITH TRANSLATOR

Maximum Signal Level -	100 MV into 50 ohms (-7 dBm)
Maximum Dynamic Range -	60 dB in 20 MHz bandwidth including feedthrough at 24 MHz
Center Frequency -	24 MHz <u>\pm</u> 0.01 MHz
Maximum Bandwidth -	20 MHz
Maximum Leakage Power (Total) -	-25 dBm
Leakage Spectrum -	More than 50 dB down from 24 MHz level at frequencies beyond <u>\pm</u> 50 kHz from 24 MHz.

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3.1.2 WITHOUT TRANSLATOR

Maximum Signal Level -	100 MV into 50 ohms (-7 dBm)
Maximum Dynamic Range -	60 dB for full 10 MHz bandwidth
Signal Band -	0 to 10 MHz

3.2 BINARY INTERCONNECTIONS WITH SCANNER

There are four different binary signals passed between the scanner and the signal processor:

1. X coordinate (horizontal range coordinate of scanner focus point).
2. Y coordinate (vertical height coordinate of scanner focus point).
3. Range scan sense signal (indicator of direction in which range scan is moving: in or out).
4. Clock signal (timing to determine discrete times at which X and Y coordinates of scanner position are sampled).

The first three signals originate in the scanner for use by the signal processor, and the fourth is generated by the signal processor for use by the scanner. The X and Y signals are ten bit words and all signals are TTL.

3.3 DIGITAL RECORDER INTERCONNECTIONS

Standard TTL binary data are supplied by the formatter unit in serial form over a single type RG-59 coaxial cable which is to be terminated in 75 ohms.

3.4 DISPLAY INTERCONNECTIONS

Connectors are provided at the rear of the signal processor for two GFE display units, one displaying X, Y, and Z data and the other displaying X, 2Y, and Z data as described in the display interface. Both connectors identical with the "signal interface connector, J701" of the GFE Tektronix type 613 display and wired to apply appropriate signals to pins, 1, 2, 4, 5, 15, 16 and 20 of these connectors.

3.5 ANALOG RECORDER INTERCONNECTIONS

Seven signal interconnections are provided: four for the record function and three for playback, as described in the display interconnection. Each connection is by means of a type BNC jack at the rear of the signal processor.

3.6 REMOTE CONTROL INTERCONNECTIONS

A connector of type similar to that for the displays is provided for the remote control function.

SECTION 4

PERFORMANCE CHARACTERISTICS

Performance characteristics not covered in the preceding sections are summarized below with appropriate comments.

4.1 VELOCITY COVERAGE RESOLUTION

The processor electronics, with the exception of the SAW delay line in the spectrum analyzer, is capable of processing an instantaneous bandwidth of 18 MHz. The delay line itself has a minimum 3 dB bandwidth of 12 MHz. The design goal for useful performance using the actual delay line characteristics is 18 MHz. Within this bandwidth, the central 6 MHz portion will provide a resolution of 100 kHz, with the resolution degrading slowly beyond this range but at least equivalent to ten percent of the input frequency. See Figure 2.

4.2 SIGNAL INTEGRATION

The detected output of the spectrum analyzer is integrated by a batch-type digital video integrator. An analog-to-digital converter at the input of the integrator provides eight bits of quantification. The A/D converter samples the spectrum analyzer output amplitude at points separated by 0.173 microseconds, corresponding to a frequency resolution interval of 104.17 kHz. The duration of the integration period provided is selectable from 0.50 milliseconds to 64 milliseconds in binary steps. Provision is made for selecting the integration time from a remote location. For this, three connections are provided at the rear of the processor such that, when the front panel "integration time" control is in the remote position, grounding one or more of these lines will select the integration time.

Velocity coverages for the five modes of operation are shown in Figures 3 and 4.

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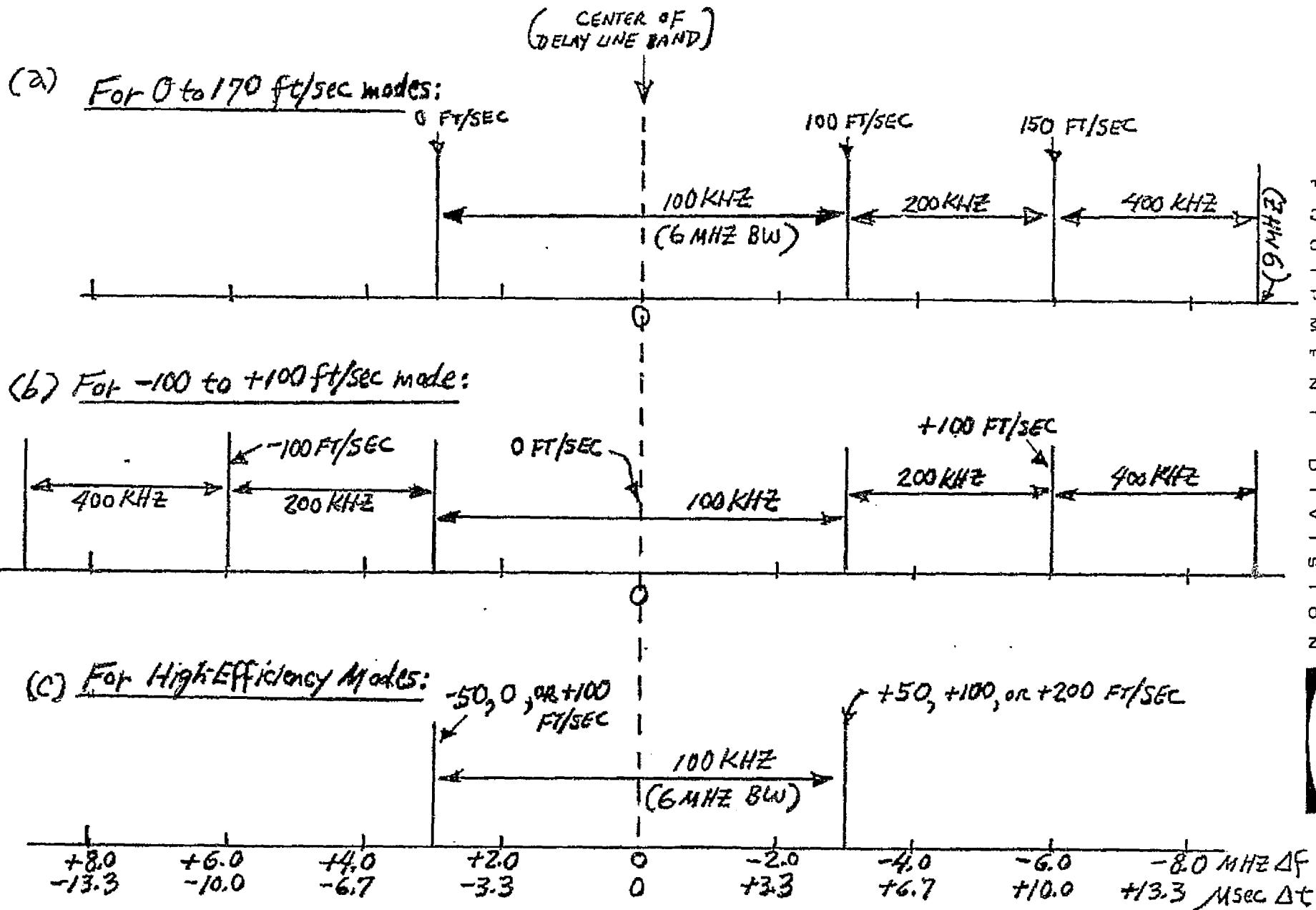
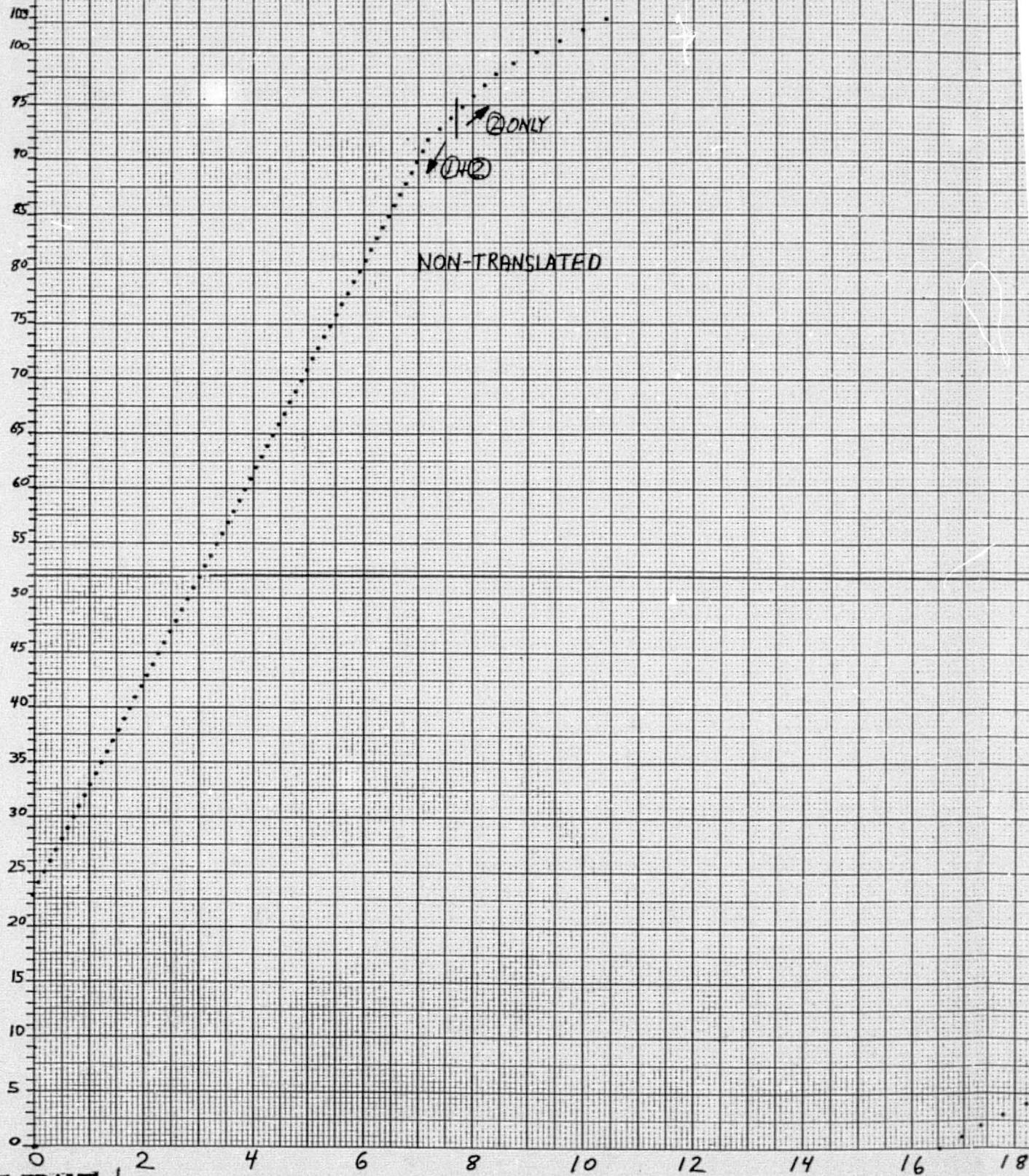


Figure 2. Spectrum Analyzer Resolution (as a function of different velocity coverage modes)

OUTPUT
CELL
NO

LVD SIGNAL PROCESSOR FREQUENCY COV

HEWLETT-PACKARD 92270-1024



FOLDOUT FRAME 1

IN

FREQUENCY COVERAGE

NOTE: CIRCLED NUMBERS REFER TO VELOCITY COVERAGE SWITCH POSITION

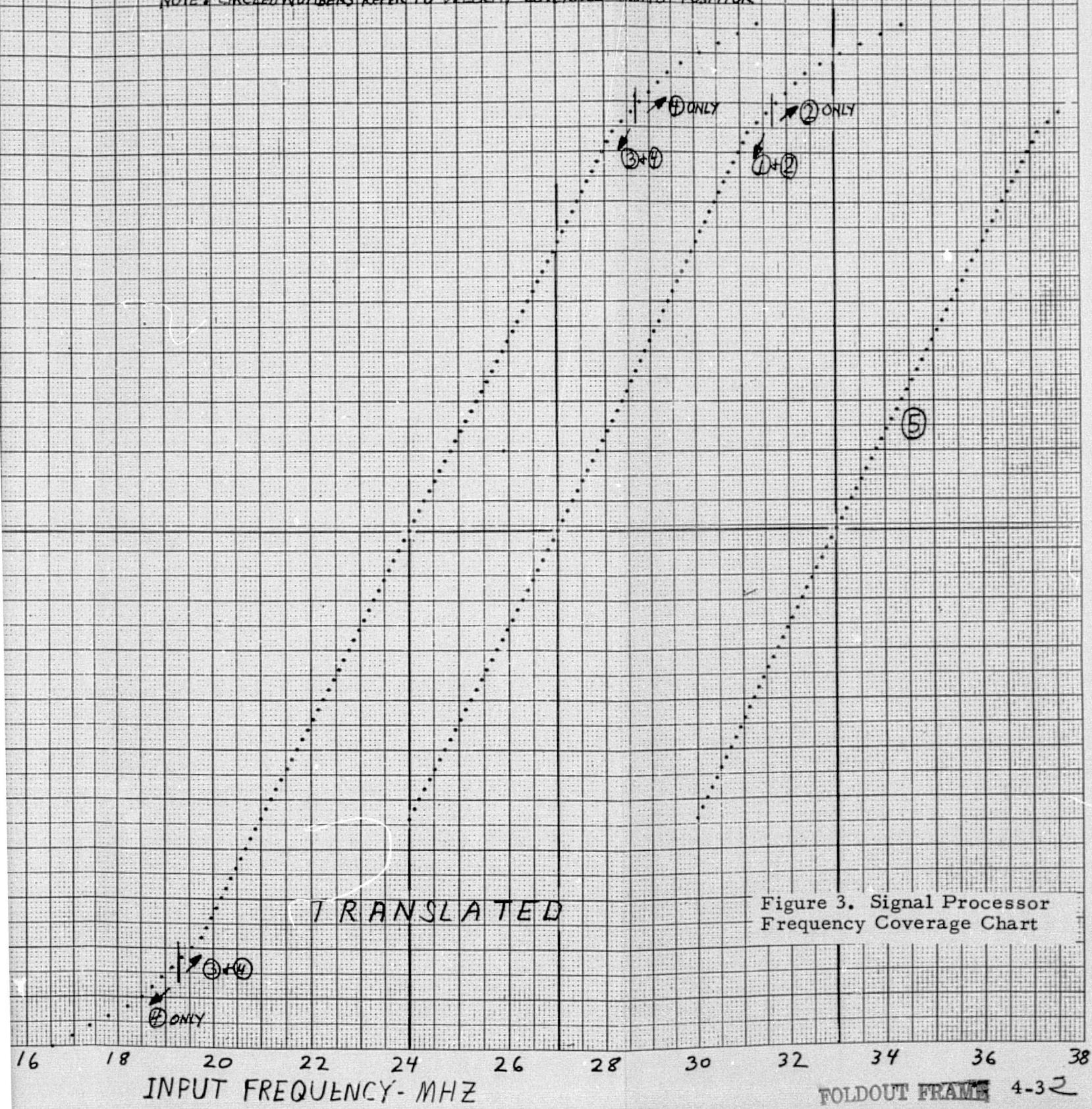
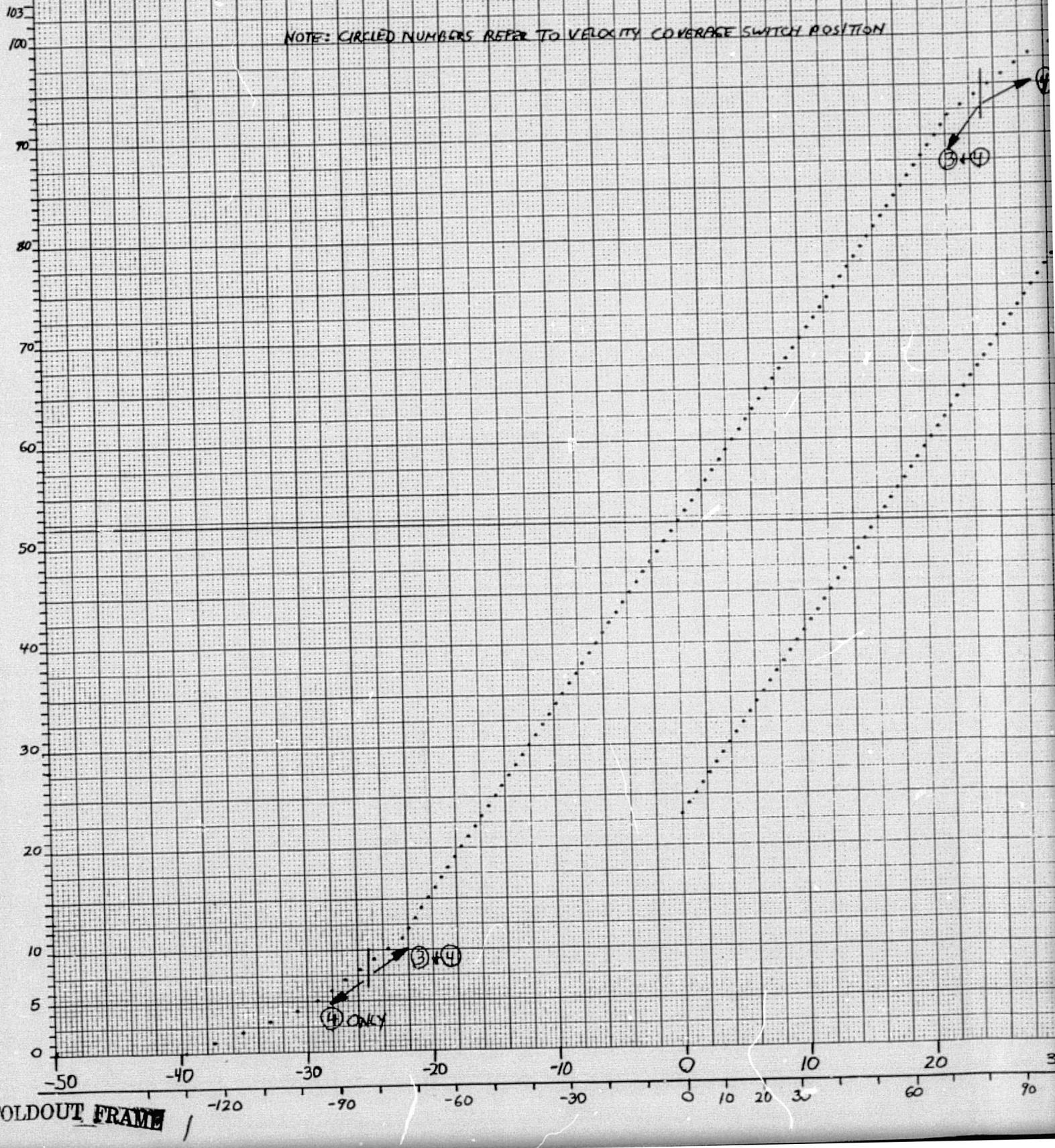


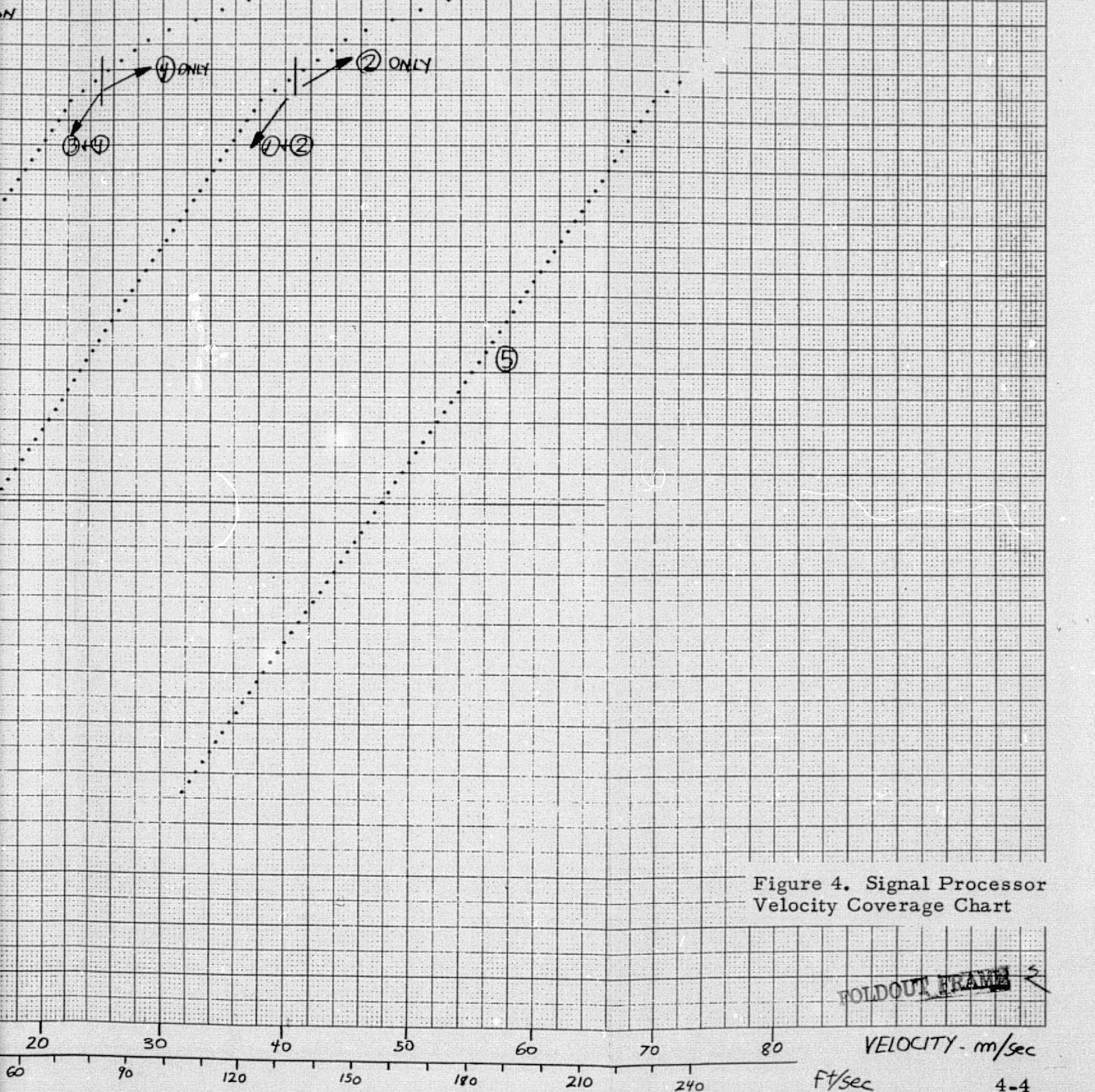
Figure 3. Signal Processor Frequency Coverage Chart

OUTPUT
CELL
NO.

LVD SIGNAL PROCESSOR VELOCITY COVERAGE



COVERAGE



SECTION 5

SUB-ASSEMBLY DESIGN

5.1 SPECTRUM ANALYZER

The spectrum analyzer receives a signal in the range between approximately zero and 34 MHz directly from a low-noise post-amplifier associated with the photo-detector in the laser-optics assembly. This signal is equivalent to a video output signal from the laser assembly for the case when the laser translator is not used and is equivalent to an IF output when the translator is used. In both cases, the spectrum analyzer treats the signal as an rf signal, separating the energy according to its spectral distribution into a number of equivalent filter-bank filters. After this frequency resolution is obtained, the output of each filter is envelope detected and it is this video signal which is converted to binary form in the succeeding spectrum integrator portion of the signal processor. The video at this point should not be confused with the video signal sometimes obtained from the laser photo-detector (when the translator is not used).

A further point of possible confusion which should be noted is that the design of the spectrum analyzer involves translating the rf input signals to other frequency ranges. This input translator circuitry should not be confused with the translator associated with the laser assembly.

5.1.1 INTRODUCTION

A block diagram of the spectrum analyzer is given in Figure 5. There are four main circuit areas in the analyzer: (1) the rf section, (2) the impulse generator, (3) the weighting circuit, and (4) the AGC circuit. Each of these is described separately below.

5.1.2 RF SECTION

The rf section arrangement is shown in the attached Figure 6. The rf section itself has four circuit function areas: input translation, frequency resolution, chirp generation, and chirp translation. The frequency resolution circuitry is the most significant. It is constrained to operate at a center

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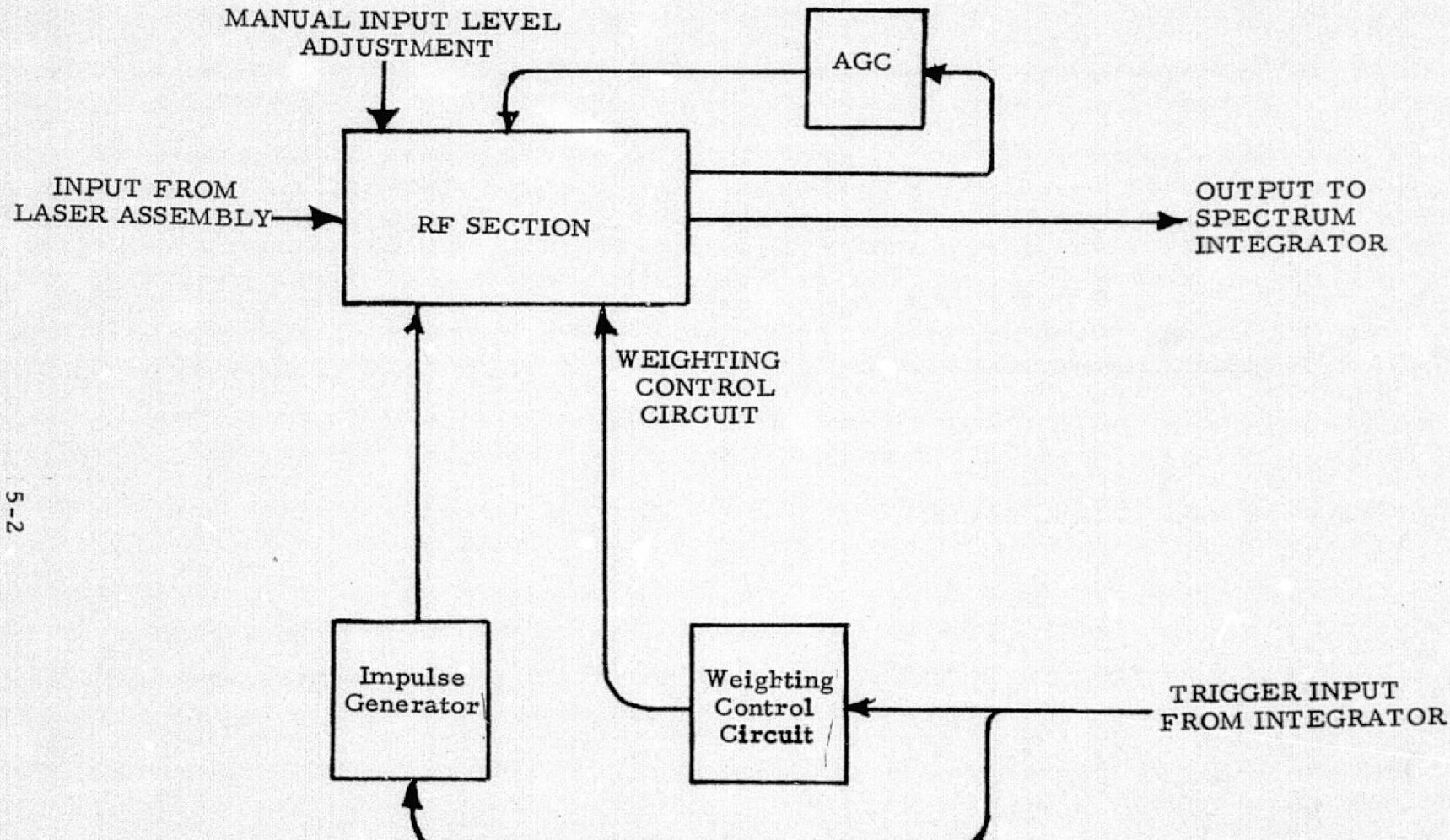
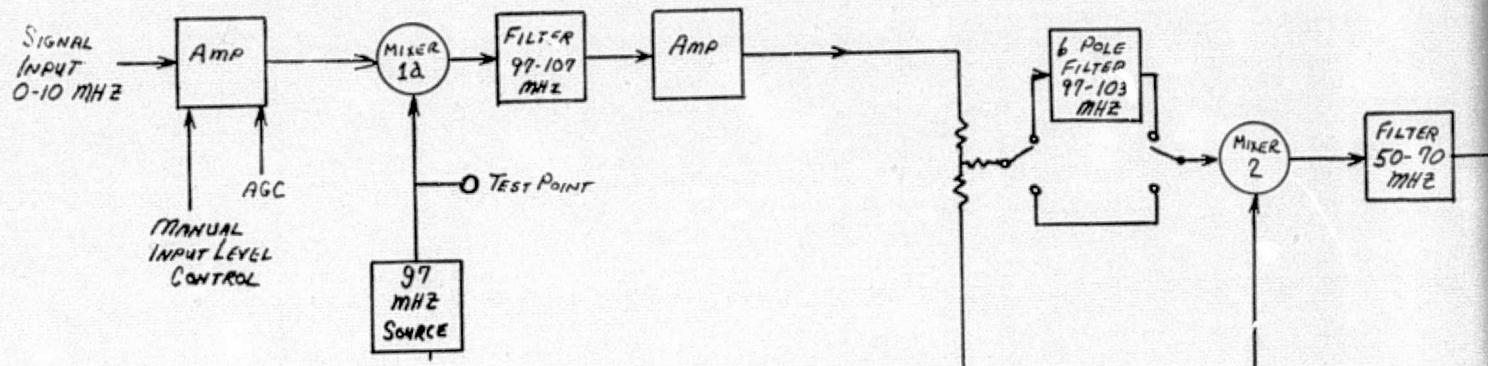


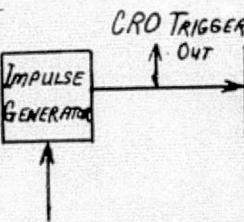
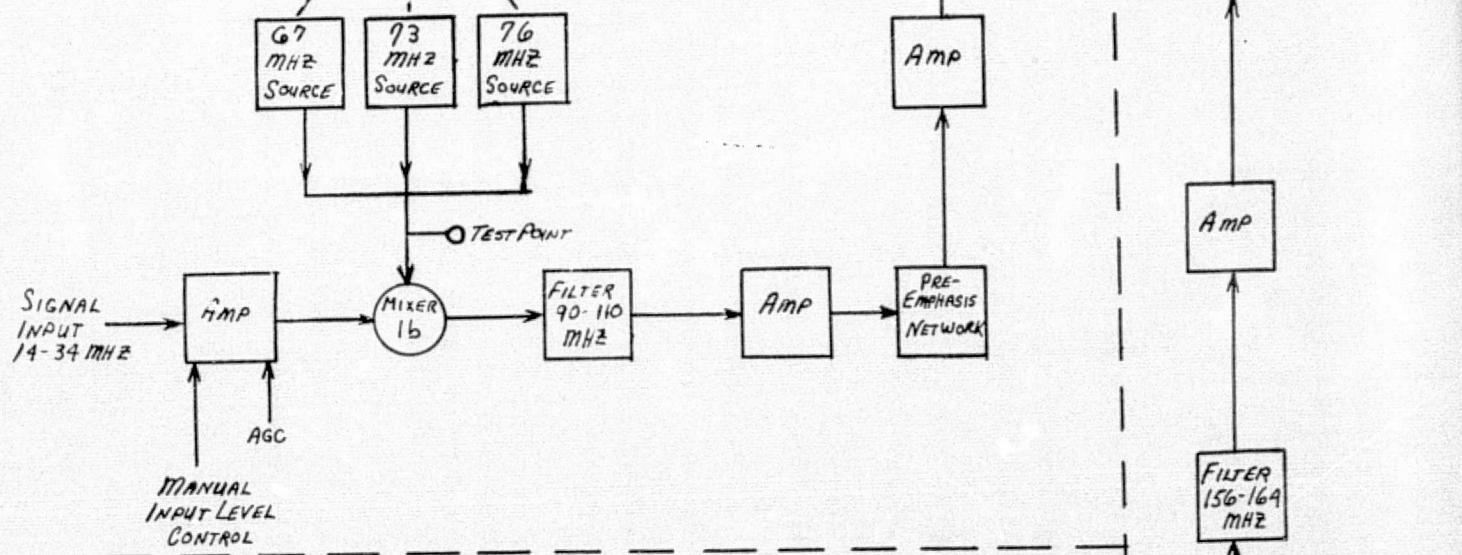
Figure 5. Spectrum Analyzer Block Diagram

INPUT TRANSLATOR 1

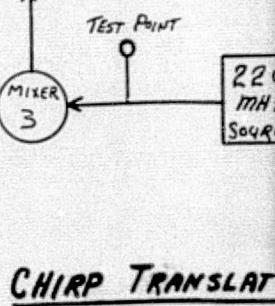


VELOCITY COVERAGE
MODE SELECTION →
(ACTIVATE ONE SOURCE)

INPUT TRANSLATOR 2



CHIRP GENERATOR



FOLDOUT FRAME

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OF POOR QUALITY

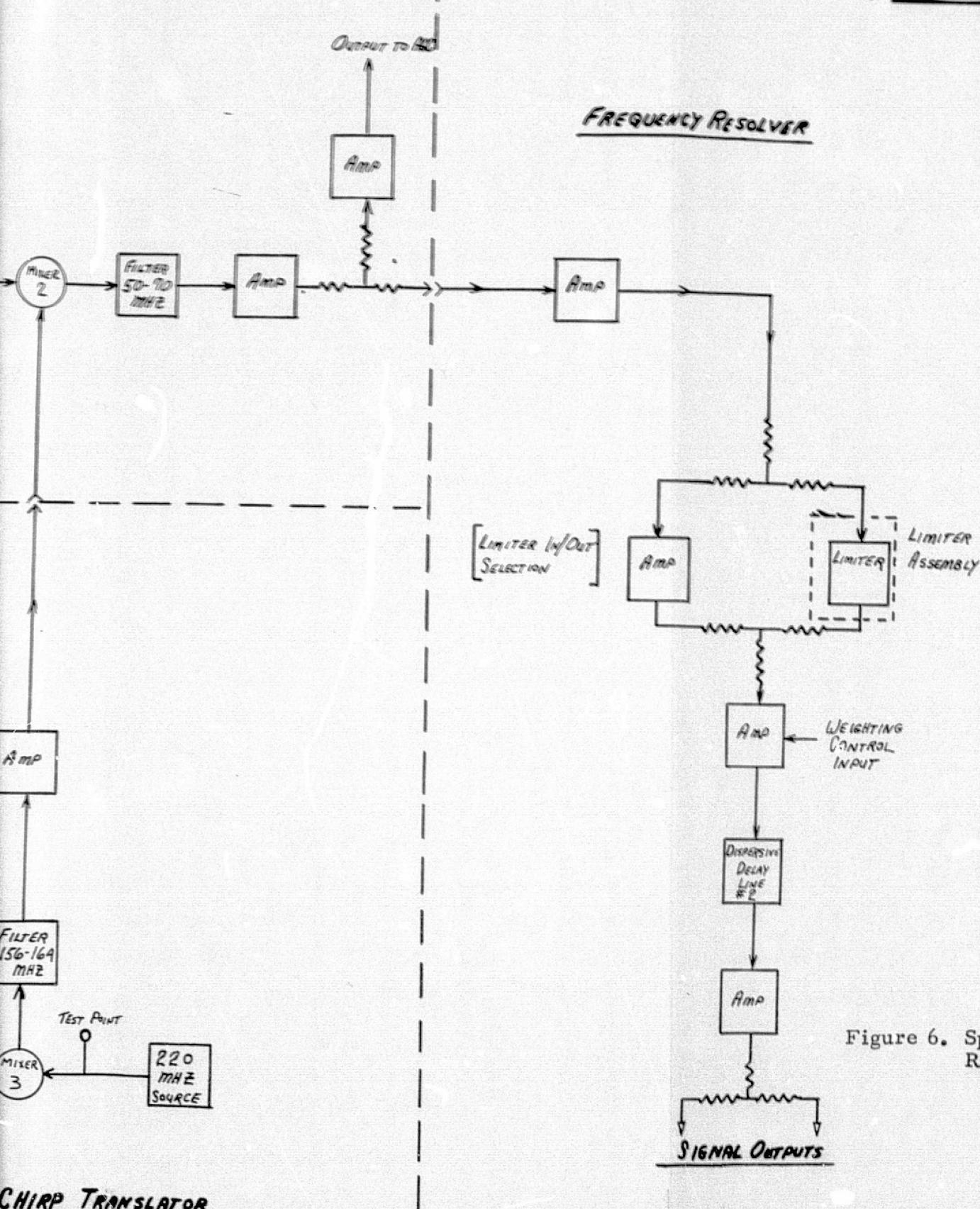


Figure 6. Spectrum Analyzer RF Section

frequency of 60 MHz by the SAW delay line characteristics and provides frequency resolution of the input signal energy by means of the frequency dispersion characteristic of the delay line. This circuitry, in combination with the input translation circuitry, determines the velocity coverage and will be capable of at least an 18 MHz bandwidth (3 dB) except for the SAW delay line bandwidth limitation. These circuit areas are discussed further below.

The chirp generation and chirp translation circuit areas are straightforward except for the choice of frequencies. The chirp is generated at 60 MHz as dictated by the SAW delay line but is translated up to a center frequency of 160 MHz in such a way that, with the input signal translated to a center frequency of 100 MHz, a 20 MHz wide signal range is produced at 60 MHz (by mixer #2) without generating spurious in-band frequency products in the various mixers which are less than 40 dB down from the desired signal.

5.1.2.1 Input Translation

The input frequencies are translated up to a frequency range at 100 MHz by means of an oscillator selection which is determined by the velocity coverage control. For example, the 0-10 MHz input range is shifted to the 97 MHz - 107 MHz range which, after frequency mixing with the 160 MHz chirp in the frequency resolution circuitry, makes the low velocity end of the range fall in the part of the SAW delay passband where the highest frequency resolution is obtained. It will be noticed that the velocity coverage cannot be permitted to go to zero as this would correspond to the 97 MHz oscillator leakage frequency. The bandpass filter characteristics following mixer 1a and the velocity gating in the velocity discriminator are designed to adequately reject this frequency, while providing low frequency coverage down to within 100 kHz (3 dB point) of 97 MHz.

For operation with the translator, one of three oscillators is used to determine the range of input frequencies which are centered in the passband of the SAW delay line. For the 76 MHz oscillator, an input frequency of 24 MHz corresponds to the center of the delay line, for 73 MHz it is 27 MHz, and for 67 MHz it is 33 MHz. These center frequencies correspond to velocities of 0, 50, and 150 feet per second, respectively.

The pre-emphasis network is used in the signal path following mixer 1b to compensate frequencies falling on the skirts of the SAW delay line when operating in velocity coverage modes requiring instantaneous bandwidths in excess of 10 MHz. It is a passive filter network designed to provide a gain versus frequency characteristic which is the inverse of the delay line characteristic within the 20 MHz processor bandwidth when used with the translator.

5.1.2.2 Frequency Resolution

The frequency resolution of the spectrum analyzer is defined essentially by the characteristics of the SAW delay line. There are two features of these characteristics of primary interest: the dispersion characteristic and the phase/amplitude useful bandwidth. The dispersion characteristic is essentially linear, being 1.67 microseconds per megahertz throughout the useful bandwidth. Thus, a shift in the input frequency being analyzed of one megahertz creates a shift of 1.67 microseconds in the position of the output signal.

The useful bandwidth which is achieved is a minimum of 12 MHz.

Beyond the SAW delay line, the bandwidth of the frequency analyzer is determined by bandpass filters incorporated in the frequency resolution circuit area. For extended coverage (wideband) operation, a 20 MHz wide bandpass filter is used, whereas for high efficiency operation, a 6 MHz (3 dB) bandwidth filter is inserted. This narrower filter is used with a short spectrum analyzer scan time to rapidly sample the input spectrum. To avoid frequency ambiguities, at this high sampling rate (15 microseconds), the filter must sharply attenuate frequencies beyond the 3 dB bandwidth. The design requirement is that frequencies separated from the center frequency by more than 1.5 times the filter half-bandwidth be attenuated at least 40 dB. A filter equivalent to a seven pole, 0.1 dB ripple Chebyshev design is required here.

The linearity of the spectrum analyzer within its 35 dB output dynamic range is determined by the "limiter in/out" switching in the frequency resolution circuit area. When the limiter is used, sufficient gain is introduced to bring the minimum signal level (noise) up to the hard limited condition. As a result, the signal power applied to the succeeding circuitry is constant regardless of the spectral content or input signal amplitude variations. The pulse compression

action of the dispersive delay line (#2) then resolves this power into a time-distributed output dependent only on the spectral content. Thus, for an input signal which is purely noise, the output of the spectrum analyzer in each velocity bin is fixed and constant, and the false alarm rate with respect to a fixed threshold is kept constant. If the input signal is strong and at a single frequency, all of the signal energy is resolved in a single velocity bin and produces a peak amplitude which is greater than that obtained for pure noise by the factor \sqrt{N} , where N is the number of filter bins. Thus for 60 bins, the dynamic range in the CFAR mode is about 18 dB.

When the limiter is not used, the spectrum analyzer provides linear operation with a useful output dynamic range of at least 35 dB.

5.1.3 IMPULSE GENERATOR

The function of the impulse generator is to create a flat spectrum over the range of 57 MHz to 63 MHz in a very short time interval. It is required that the generator be able to operate at a PRF of up to 70 kHz.

The selected approach is to use an avalanche transistor which is capable of producing a pulse of about five nanoseconds duration and 30 volts magnitude into 50 ohms. The overall circuit (Figure 7) consists of a delay generator, a gate generator and the avalanche transistor circuit. The delay generator delays the spectrum analyzer trigger such to synchronize the start of the chirp waveform with the start of the velocity scan period in the spectrum integrator. This delay is variable in order to adjust for residual time delays in the spectrum analyzer section. The gate generator produces a pulse to drive the avalanche transistor.

5.1.4 WEIGHTING CIRCUIT

As a means of reducing the high time-sidelobes that would generally be produced at the output of the spectrum analyzer ($\frac{\sin x}{x}$ waveform) time-amplitude weighting is employed. This is accomplished by modulating the gain of an amplifier just preceding the output dispersive delay line. The amplitude weighting to be used is a cosine-squared plus pedestal (see Figure 8) with a pedestal height of eight percent (Hamming weighting). The actual shape of the modulation waveform will be governed by the voltage-gain transfer characteristics of the amplifier.

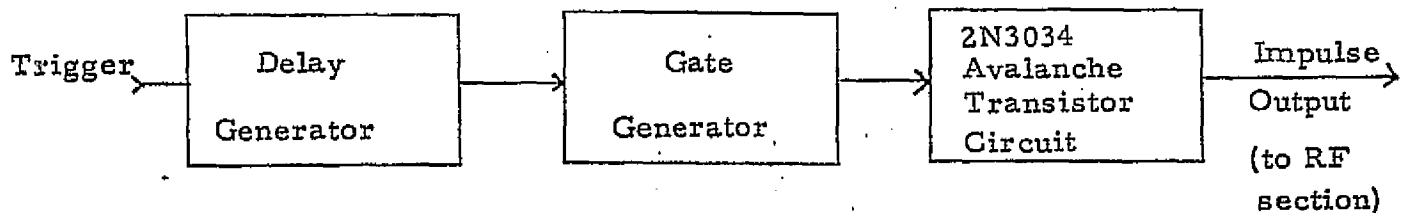


Figure 7. Impulse Generator Arrangement

The method for producing the modulation waveform can be seen from the block diagram in Figure 9. The read only memory (ROM) is a field-programmable, 32 X 8 memory with an address-to-output access time of 50 nsec maximum and will be programmed for half the modulation waveform (5 μ sec) in 30 words (including zero). The second half of the waveform is generated when the count control detects the maximum sample count and causes the counter to address back down to zero. The eight bit output of the ROM allows for small enough quantization so as to produce a relatively smooth waveform. The trigger delay is required to make the weighting function coincide in time with the chirp waveform in the rf section (see Figure 9A).

5.1.5 GAIN CONTROL CIRCUIT

The signal level is controlled by a combination of manual gain control and automatic gain control both applied to an FET amplifier at the input of the spectrum analyzer. The manual control is used to regulate the day-to-day variation in signal level over a range of about 30 dB. This is accomplished through a simple potentiometer arrangement on the amplifier voltage.

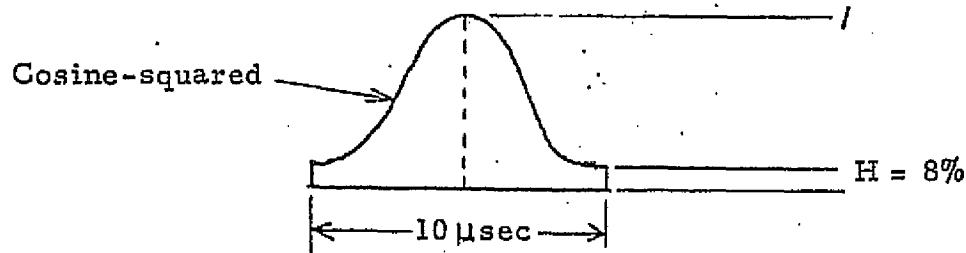


Figure 8. Hamming-Weighted Chirp Waveform

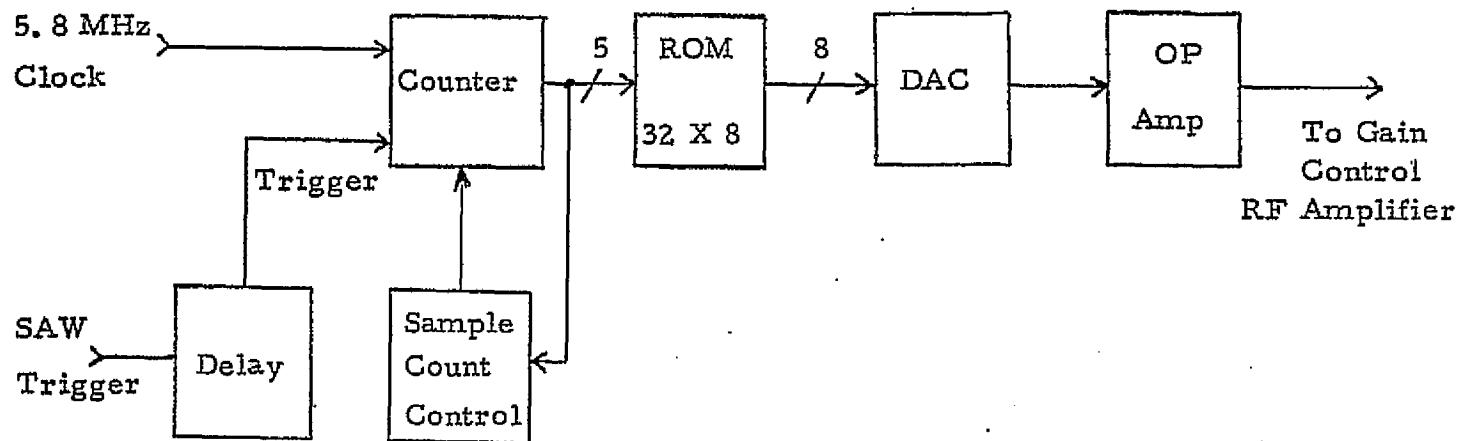
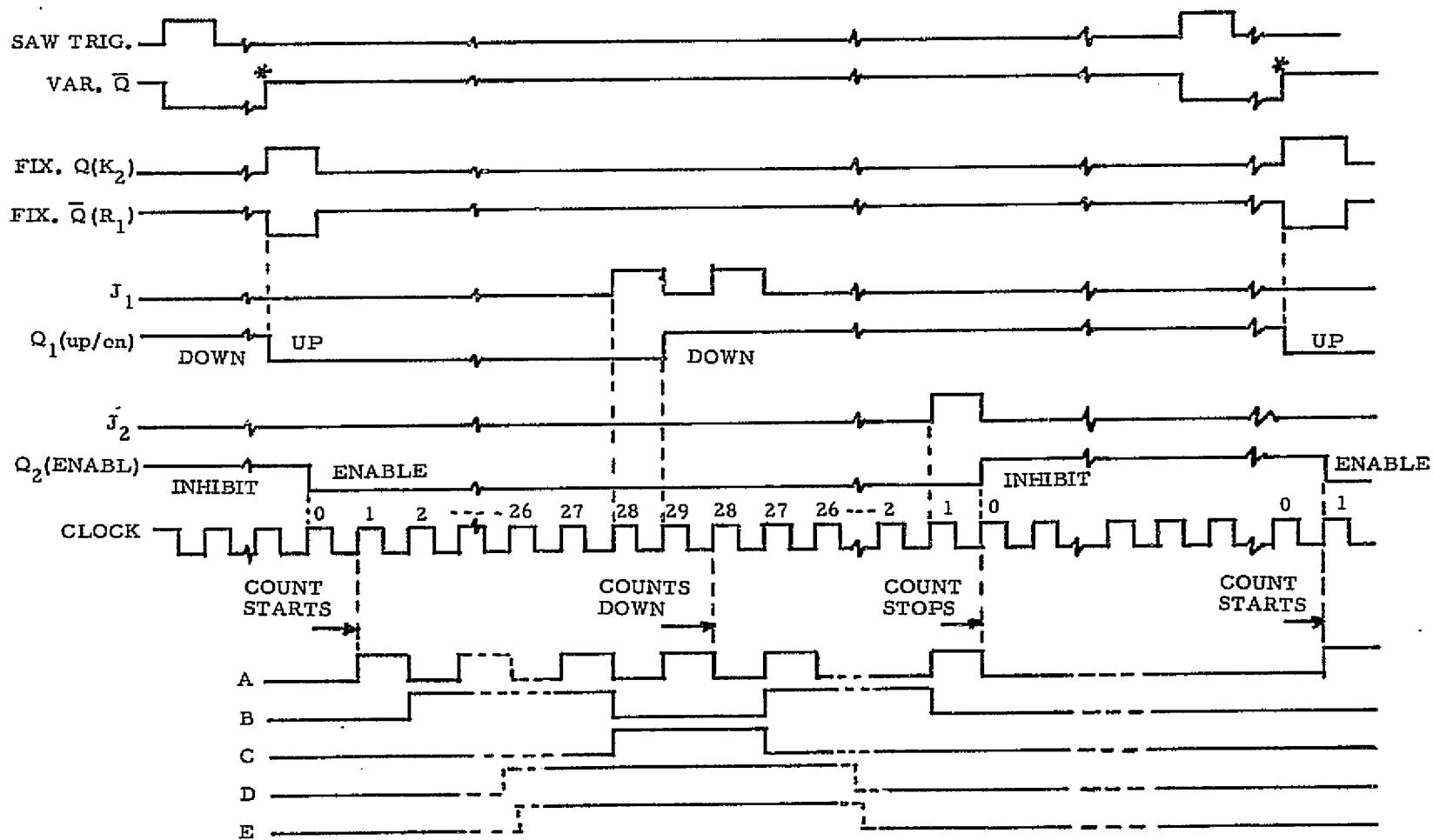


Figure 9. Block Diagram of Weighting Function Generation



*VARIABLE DELAY: 14-21 μ sec for Extended Coverage Mode
2.5-3.8 μ sec for High Efficiency Mode

Figure 9a. Weighting Control Timing Waveforms

The automatic gain control (AGC) will regulate short-term variations, such as those arising from airplane exhaust or a rainfall and will cover a dynamic range of about 30 dB also. The AGC circuit uses a detector to monitor the signal amplitude in the rf section and from this derives a dc control voltage which is applied to the amplifier at the input of the rf section.

The signal level in the rf section at which point the AGC becomes effective to keep the signal constant is adjustable by means of an "AGC threshold" potentiometer. This determines a reference voltage against which the output of the AGC detector is compared.

The time constant chosen for the AGC circuit is approximately one minute. This is desirable to average the signal variations occurring over a complete elevation scan of the scanning system. To expedite adjustment of the manual gain control as well as the threshold control, an AGC time constant switch is provided to shorten the time to about one second.

5.2 SPECTRUM INTEGRATOR

The spectrum integrator processes the 60 MHz i-f output of the surface-acoustic-wave spectrum analyzer to provide amplitude versus doppler-frequency information with decreased data rate and increased signal-to-noise ratio. Operation of the unit is described briefly in the following paragraph and in the succeeding sections, each of which applies to one of the three circuit cards.

The integrator generates a periodic spectrum-analyzer-trigger signal, initiating a frequency scan or spectrum analyzer cycle. Within the integrator, the resulting i-f output is amplified, envelope detected, and converted at a 5.76 MHz rate to a doppler-velocity-ordered time series of 90 or 180 input cells per cycle, wherein each cell contains an eight bit binary word representing amplitude. Batch integration is performed by maintaining one running-sum per cell, updated once per cycle, in an accumulator. When a number of successive cycles have been accumulated such that the selected integrated time (0.5 to 64 milliseconds) has elapsed, the accumulator contents are transferred to an output memory. During the following integration period, the information in the output memory appears serially as the integrator output at a rate inversely related to integration time.

5.2.1 A/D CONVERTER CARD

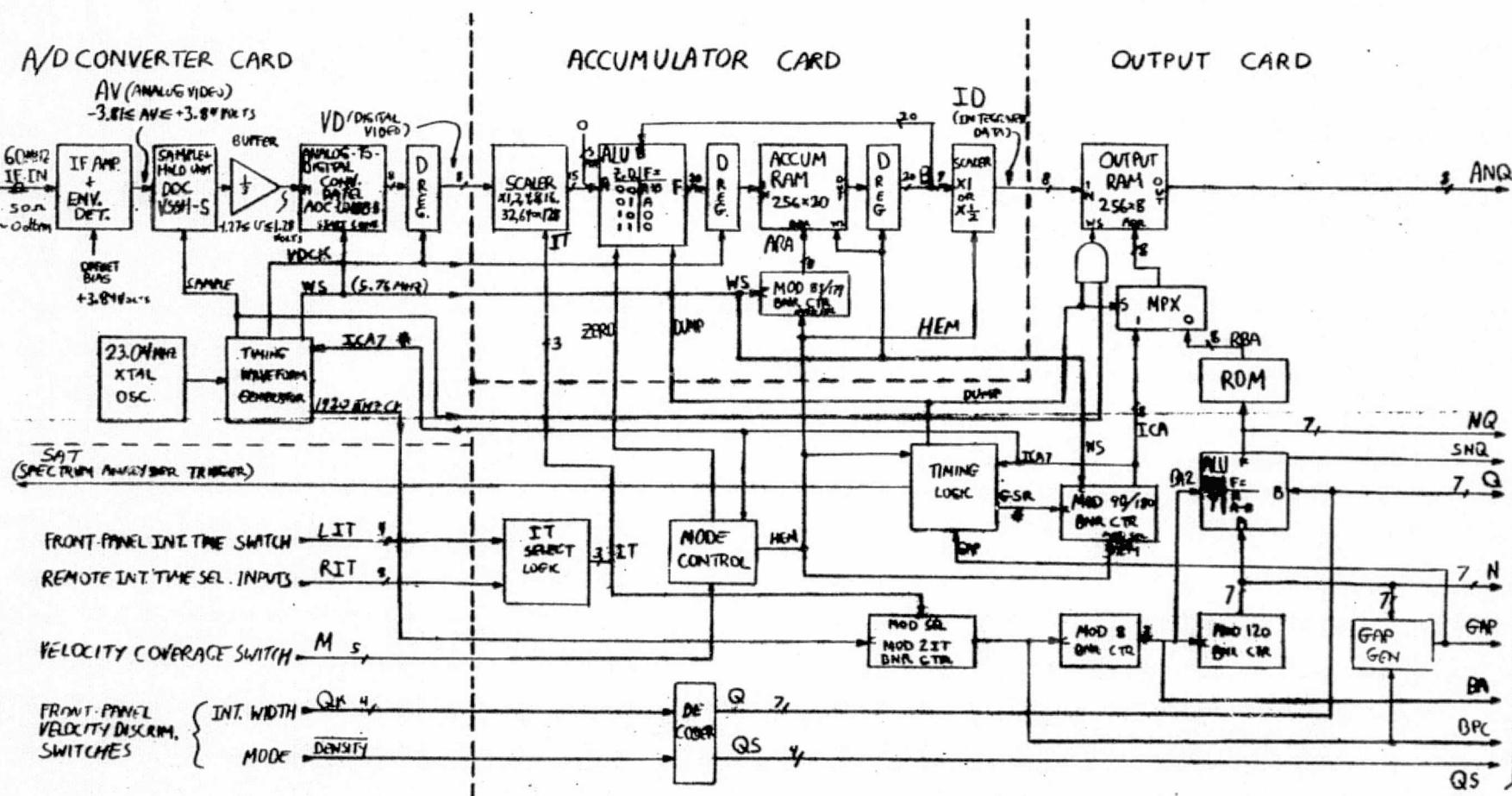
Figure 10 is a block diagram of the spectrum integrator, shown partitioned according to circuit card boundaries. The A/D converter card is driven by a 60 MHz i-f signal from the spectrum analyzer which must provide a maximum power of approximately 0 dBm into a 50 ohm load. The envelope detector output ranges from -3.81 volts at this maximum input level, to +3.84 volts at zero signal; the bandwidth here is about 3 MHz.

The sample and hold unit, required to hold the A/D converter input constant during its two-step conversion process, has a high impedance input. The sample and hold unit has insufficient output current capability to drive the A/D converter directly, so a high-slew-rate hybrid integrated-circuit buffer has been included. Attenuation in the buffer output decreases the voltage range to -1.27 to +1.28 volts at the A/D input. This attenuation permits most of the range of the sample and hold unit and buffer to be utilized, thus minimizing effects of distortion and offset in these devices.

The two-step conversion process involves determination of the four most significant bits in a parallel four bit converter, followed by a subtraction of an analog version of this result from the input voltage (still unchanged because of the sample and hold unit) to determine the four least significant bits. A timing diagram, appearing in Figure 10a, illustrates the operation of the A/D converter. The A/D digital output is loaded into a register at the zero-one transition of VDCK, which occurs at a time when all eight bits are valid for the preceding sample. The sampling range is 5.76 MHz and the total throughput delay is about 200 nsec.

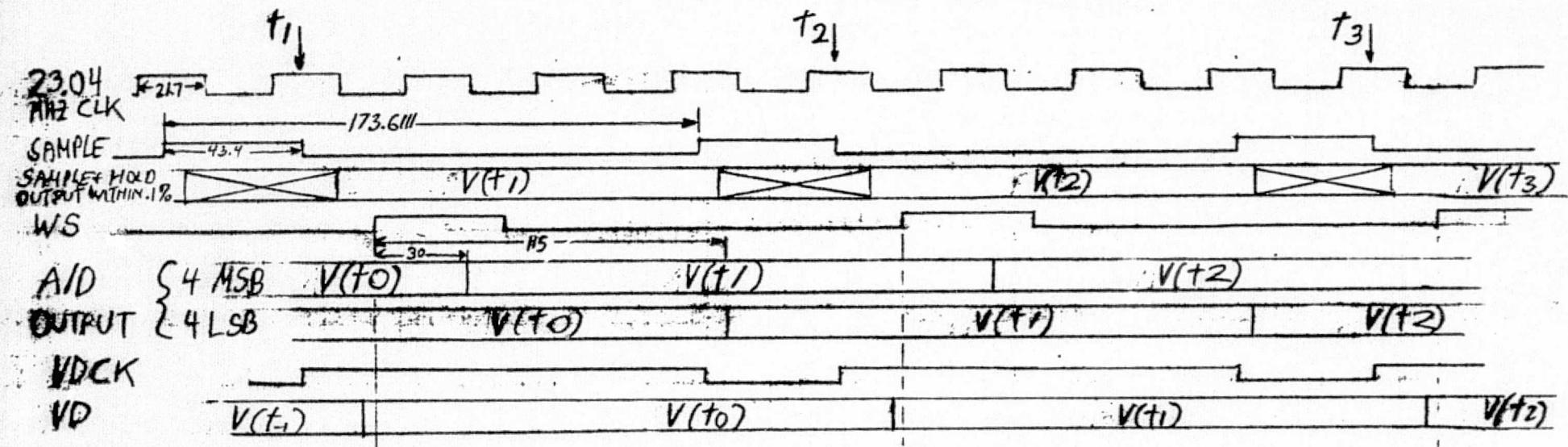
All high-speed clocks required in the integrator, for example, VDCK mentioned above, are derived from a 23.04 MHz crystal-controlled oscillator driving a timing waveform generator which is implemented using Schottky-clamped TTL integrated circuits.

The conversion rate of the A/D converter is a limiting factor in system performance, and therefore deserves further discussion which might aid attempts at extending system performance; if, for example, SAW delay lines having finer resolution were installed in the spectrum analyzer.

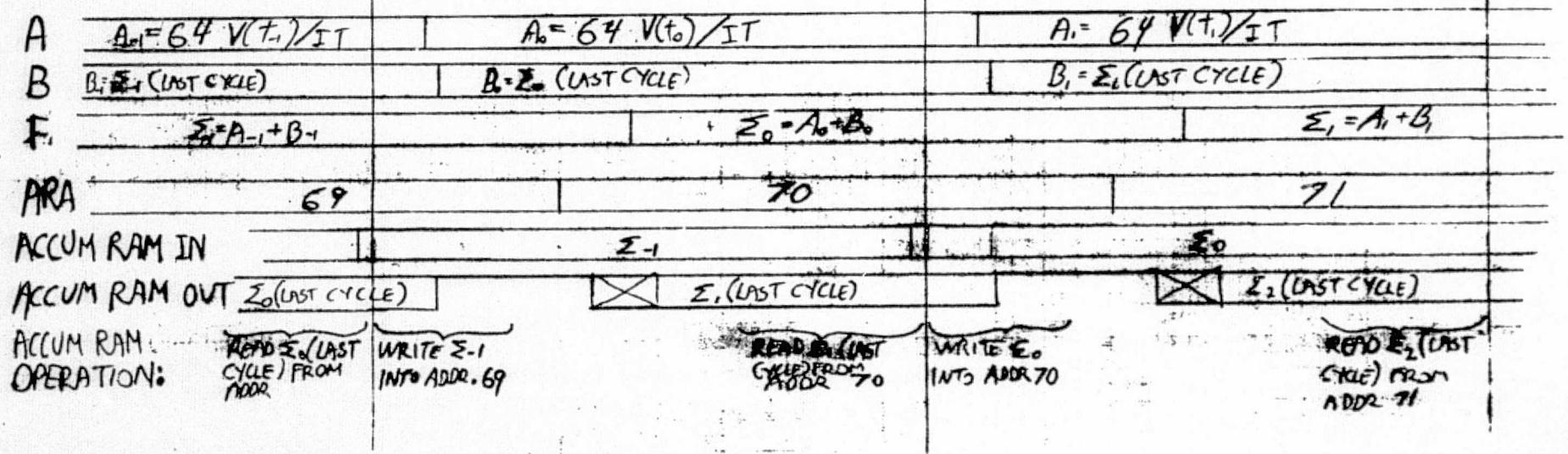


* These feedback signals are used to ensure proper phase relationships among all of the counters

Figure 10. Spectrum Integrator Block Diagram



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Figure 10b Accumulator Waveforms

NOTE: ALL TIMES IN NANOSEC

The A/D Converter limits the conversion rate to 10^7 words/second; time must also be allowed for sample and hold acquisition. Table II lists extended performance obtainable by methods which involve various levels of effort.

Only Method 6 shows promise of approaching 10^7 conversions per second. Here, a delay line permits decreasing the amount of time during which the sample and hold output must remain stable, thus permitting the four MSB converter to begin operating on a new sample before the four LSB determination has been completed.

TABLE II
A/D Conversion Rate Extension

<u>Description of Changes to Existing Design</u>		<u>Conversion Rate</u>
1.	None	5.76 MHz
2.	Increase crystal oscillator frequency	6.15 MHz
3.	Alter Timing, 2	6.75 MHz
4.	Substitute faster sample and hold unit--VSSH-F*, 3	8.0 MHz
5.	Substitute faster sample and hold unit to be announced by DDC, 3	~8.0 MHz
6.	Add delay line and attenuator, 3	~10.0 MHz
*	Subject to degradation in linearity to that of a six bit converter.	

5.2.2 ACCUMULATOR CARD

The arithmetic and accumulator-memory circuitry of the integrator is located on the accumulator card. In order to normalize the output, the incoming eight bit digital video is multiplied by 64/IT in the scaler. Because the integration time, IT, is always a power of two ranging from 0.5 to 64 milliseconds, this multiplication is simply an appropriate shifting of bits. The scaler is implemented with straight forward combinational logic available as MSI integrated circuits (Signetics 8243).

The actual addition is performed in ALU (arithmetic logic units) with look-ahead carry generators (Texas Instruments SN 74181 and SN 74182) in order to obtain adequate addition speed over 20 bits. The function inputs of the ALU provide a convenient means of disabling addition during the "dump" cycle to be described and to zero the accumulator when required. Twenty bits are required in the accumulator to accommodate sums as large as 2^{20} which could be encountered in the situation where IT is 64 milliseconds and a large amplitude is present in a cell for the entire integration period.

Selection of an implementation for the accumulator memory presented some problems because of the 5.76 MHz rate. Most conventional integrators using P-channel MOS shift registers operate only to about 2 MHz. Faster complementary MOS registers of 64 bit length are available; however, they only attain their speed with high supply voltages. In this case, the arithmetic circuitry, too slow if implemented in CMOS, must be TTL; hence, the required level interface circuitry adds cost, delay and complexity which cancels any advantage of CMOS. Use of high-speed TTL random-access memories permits flexibility not possible with fixed length registers, but with a conventional read-add-write cycle at each RAM address, operation at 5.76 MHz is possible only through use of costly Schottky-clamped ALU circuits. The approach which was chosen for the accumulator card is to emulate an M bit shift register using the RAM along with two edge-triggered D type registers as shown in Figure 8. Here, the ARA (accumulator RAM address) comes from a binary counter of modulo M-1, where M is the total number of input cells (90 or 180). Timing is depicted in Figure 10b and Figure 11, where it can be seen that the sum of a

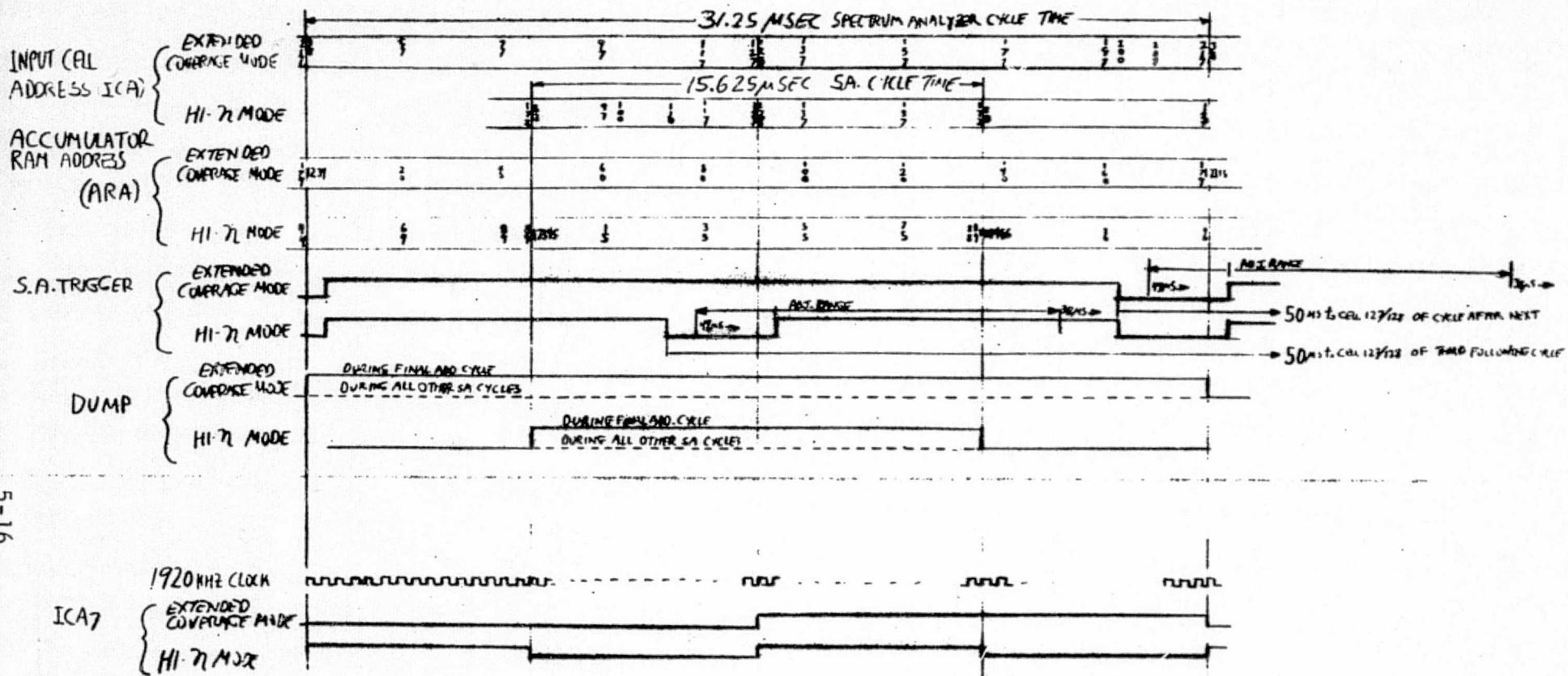


Figure 11 INTEGRATOR INPUT TIMING

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given cell is not written back into the same ARA from which it was read, but into the next greater ARA. The maximum attainable rate is limited by the greater of RAM read-write cycle time or D-register set up and delay time plus the ALU add time, not by the sum of all of these as is the case with a read-add-write cycle. With a Fairchild RAM (93410) and conventional TTL registers and ALU, the accumulator should operate at a minimum of 6.4 MHz. Substitution of Schottky-clamped ALU and registers extends this limit to the vicinity of 11 MHz.

It has been mentioned several times that there are 90 or 180 input cells per spectrum analyzer cycle. Reference to Figure 11 will reveal that these numbers correspond to high efficiency or extended coverage modes having 15.625 or 31.25 microsecond S.A. cycle times, respectively. In the high efficiency mode, there are 64 S.A. cycles per millisecond, versus 32 per millisecond in the extended coverage mode. Each velocity coverage, as selected at the front panel, enables one or the other of these modes. The scaler which follows the accumulator RAM corrects for mode changes so that the output remains normalized. Only the eight most significant bits are included in the output.

5.2.3 OUTPUT CARD

After the accumulator has operated for the appropriate number of spectrum analyzer cycles, listed in Table III as a function of integration time, a DUMP signal one SA cycle time in duration is generated by sequential logic circuitry on the output card. This signal, which is illustrated in Figures 11 and 10, causes the contents of the accumulator RAM to be transferred to the output RAM (see Figure 10). During DUMP, the ICA (input cell address), always synchronous with the SA cycle, is applied to the output RAM; while the B input of the accumulator ALU is disabled to prevent the final sums from re-entering the accumulator RAM. Generated along with DUMP are the spectrum analyzer trigger and other timing signals. Figure 11 shows that the exact timing of the S.A. trigger is continuously adjustable (by card-mounted trimpot) over a limited range.

TABLE III
SPECTRUM ANALYZER CYCLES - INTEGRATION TIME

Inputs for Remote Integration Time Selection*			IT (Integration Time)-Msec	No. of Spectrum Analyzer Cycles per IT	
RIT ₂	RIT ₁	RIT ₀		Extended Coverage Mode	Hi- η Mode
0	0	0	0.5	16	32
0	0	1	1	32	64
0	1	0	2	64	128
0	1	1	4	128	256
1	0	0	8	256	512
1	0	1	16	512	1024
1	1	0	32	1024	2048
1	1	1	64	2048	4096

* "0" Means wire grounded, "1" Means wire open. These inputs are ignored unless integration time switch is in its "Remote" position.

A diagram illustrating the output timing of the integrator appears in Figure 12, which includes a single frame or integration period. The data present at the output during this period is that which was integrated during the preceding period, having been entered into the output RAM during the dump interval. The dump operation always occurs at the beginning of the gap, during which no valid data appears at the integrator output. The portion of the gap interval occupied by the dump signal, inversely related to integration time, is 50 percent at 0.5 millisecond integration time. This organization thus permits integration times as short as 250 microseconds, where the entire gap is occupied by the dump interval.

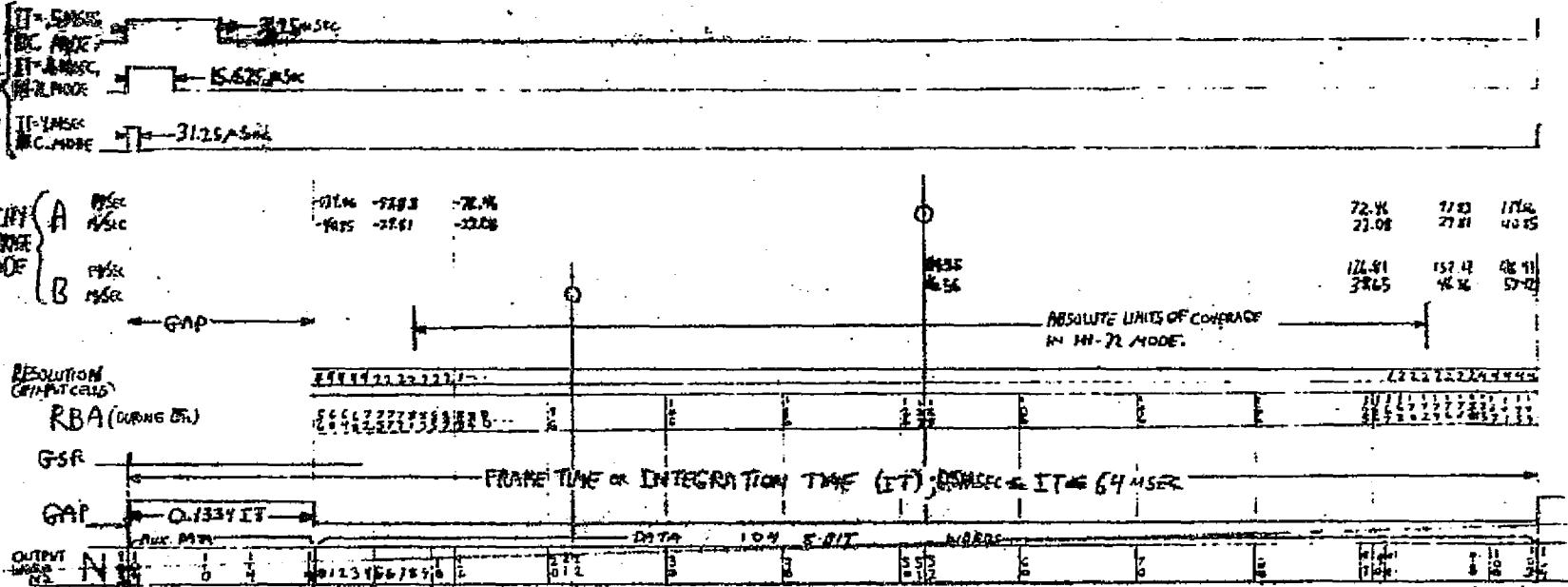
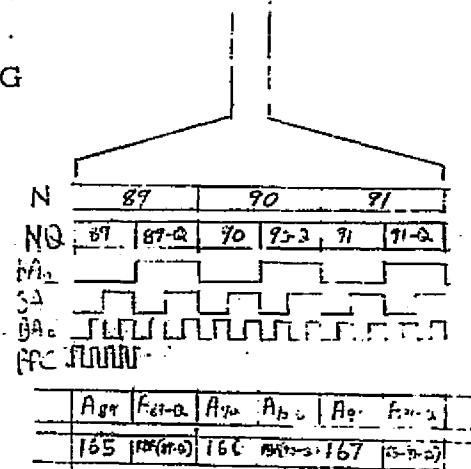


Figure 12 INTEGRATOR OUTPUT TIMING



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Some of the 90 or 180 input cells contain marginal data because of limitations in spectrum analyzer performance near the bounds of its coverage. In order to minimize the output rate of the integrator, the sampling interval (expressed in number of input cells) is increased in regions where spectrum analyzer resolution is expected to be degraded, and sampling is not done at all where no useful information is to be found. The ROM (read only memory - see Figure 10) generates the RBA (read-back address) to address the output RAM for each output word number N, as shown in Figure 12, which also shows corresponding doppler velocity coverages for reference. This approach is somewhat wasteful of memory, since 180 cells are stored in a 256 RAM and only 104 are actually outputted. It is justified because the sequential logic design is simplified, the possibility of increasing the number of output cells or altering the read-back pattern does not require additional memory, and the next-smaller memory size is inadequate to be practical in this application.

Width integration, or averaging over Q output cells where Q is selectable at the front panel, is performed in the velocity discriminator. In order to minimize data storage requirements there, the integrator output RAM is accessed twice during each output cell interval. Figure 12 shows that during the first half of each interval, the output ANQ is A(N), whereas during the second half it is A(N-Q). Decoding of QK, from front panel velocity discriminator switches, is also performed on the output card.

Output timing signals and addresses are obtained by frequency division, programmable by integration time, of a 1920 kHz square wave obtained from the A/D converter card.

When the front panel velocity coverage switch is turned to a position requiring the high efficiency mode, the unused output cells must be zeroed to avoid confusing the velocity discriminator. The mode control logic performs this function by generating the HEM and ZERO signals in proper sequence.

5.3 VELOCITY DISCRIMINATOR

The velocity discriminator card (Figure 13) performs cell-to-cell integration of spectral amplitudes and performs two methods of determining signal presence for purposes of gating the display. The first of these methods (density mode) gates the display on when the amplitude exceeds the amplitude threshold (A_t) and velocity threshold (No) at more than a selected minimum number of cells (ΔN). With this detection method, no cell-to-cell integration occurs. The second signal detection method includes cell integration and consists of finding the velocity cell at which the integrated amplitude peaks. If this highest amplitude peak exceeds the amplitude threshold, the display is gated. The velocity cell at which the peak occurred is supplied as an output to the display.

The moving window integrator takes the sum of the amplitudes of Q contiguous cells. Values of Q available are 1, 2, 3, 4, 6, 8, 12, 16, 24, 48, and 64. At each cell (N), the integrator receives two inputs serially: the first input is the amplitude of cell N , and the second is the amplitude of cell $(N-Q)$. The cell N amplitude (A_n) is added and the $(N-Q)$ cell amplitude (A_{n-Q}) subtracted from the contents of the accumulator. At the end of this process, the accumulator output is the sum of the last Q cells. In the case that Cell N (or N minus Q) lies below the velocity threshold, its amplitude is not added (or subtracted) from the accumulator. The subtraction of A_{n-Q} from the accumulator is also deleted when N minus Q is negative ($SNQ = \text{zero}$).

To normalize the integrator output the accumulator output is divided by a power of two, and, in the cases where Q is not a power of two, the amplitude threshold is multiplied by 1.5.

Concurrent with the amplitude inputs, N and $(N-Q)$ are received serially. These input addresses are offset by the address at which the velocity is zero. Half the integration width ($Q/2$) is then subtracted from the offset address to compensate for the delay through the integrator. This corrected velocity is stored in a register whenever a new amplitude peak is found.

The peak storage circuit supplies a detection output for each frame indicating that the amplitude threshold has been exceeded at one or more cells during that frame. The density counter represents the number of cells at

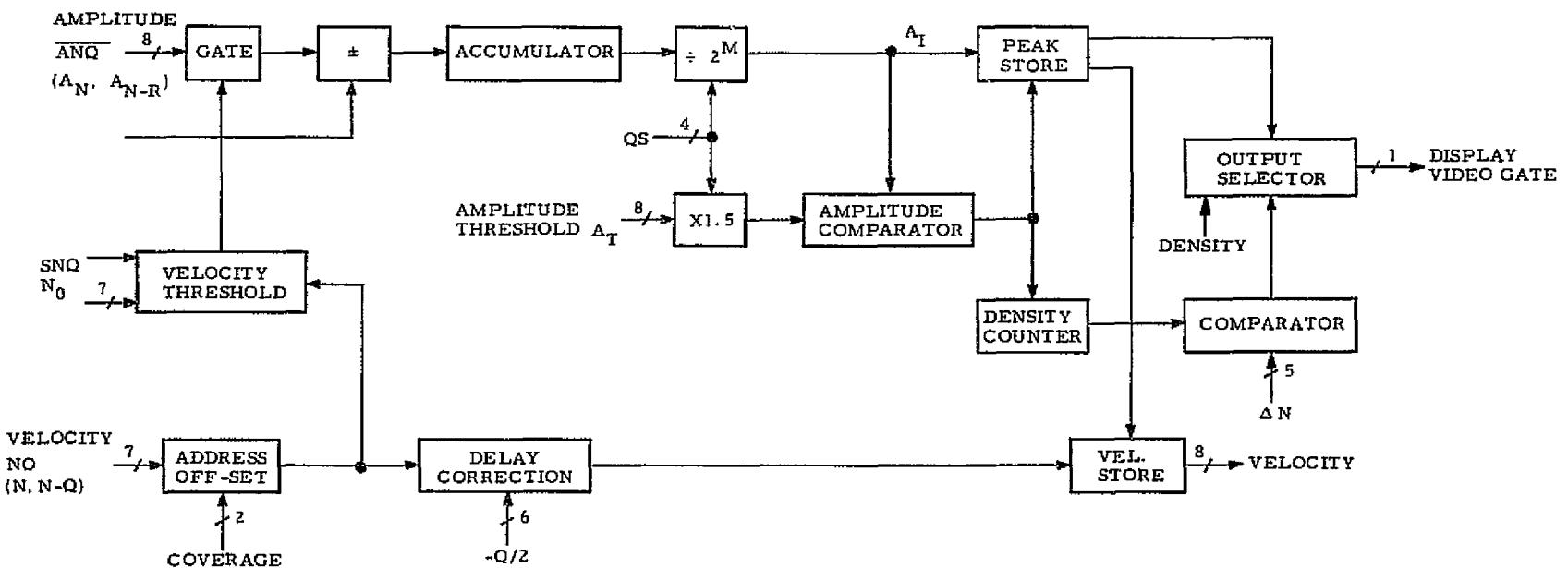


Figure 13. Velocity Discriminator

which the amplitude threshold is exceeded. The counter output is compared to ΔN to supply the detection output in the density mode. The display gate is selected from these two detection signals on the basis of mode.

5.4 DISPLAY INTERFACE

5.4.1 FUNCTION

The function of the display interface circuitry is to provide the necessary signals for displaying the signal processor output on a Tektronix 613 bistable storage display. The display is of the range-height indicator type. The display sweep tracks the scanning of the beam by means of inputs from the scanner. In its most basic form, the display is simply unblanked whenever minimum signal conditions are met. Two operating modes, providing two alternate methods of indicating velocity, and two test modes are employed. A holding state is also included in which the current contents of the display held and no new display data can be written. Display size parameters are listed below.

Scale Factor	X Coverage (Meters)	Y Coverage (Meters)	Scale Factor (Meters/cm)	2Y Coverage (Meters)	2Y Scale Factor (Meters/cm)
1	60 → 600	0 → 405	27	0 → 202.5	13.5
2	60 → 420	0 → 270	18	0 → 135	9
3	60 → 240	0 → 135	9	0 → 67.5	4.5

5.4.2 MODES

Line Width Modulation - The sweeping of the x and y during an unblanked integration period produces a line segment on the display. In this mode, the width of the line is proportional to the velocity for that period. This widening is accomplished by adding in-phase and quadrature sinusoidal signals (Δx and Δy) to the display coordinates. These sinusoidal signals are amplitude modulated by the velocity input to provide the velocity dependent line width.

Vector - This mode is for use with scanning patterns for which the range-sweep rate is large compared to the elevation (angle) sweep rate. For these patterns, the direction of an unblanked line segment is the same as the direction of the velocity. The unblanking gate for this mode has a duty cycle proportional to velocity. To provide a reference for normalizing these vector amplitudes, dots are generated by pulsing the Δx and Δy signals for a short interval in the middle of the integration period. With these dots, the sense of vectors can be displayed by gating the unblanking on only during half the integration period. The half inside the dot would designate velocities away from the laser. This sense display feature will be available as an option.

Line - This is a test mode in which the Δx and Δy signals are inhibited and the display is unblanked at all times. When used with coordinate inputs (x and y) from the scanner, the entire scan is traced on the display. This mode can also be used in conjunction with the test counters to produce lines or rasters for adjusting display size, offset, and brightness.

Dot - This test mode is the same as the line mode above, except that the Δx and Δy signals and the unblanking are pulsed only during the dot time interval in the center of each integration period. This mode is useful in adjusting dot size and checking display and scan linearity.

5.4.3 DISPLAY BUFFER CARD

Figure 14 is a block diagram of the Display Buffer. It consists of three basic functional blocks. The video control circuit generates display unblanking. The co-ordinate delay circuit delays the scanner co-ordinates to match the video delay through the processor. Circuitry to provide the necessary timing signals is also included.

VIDEO CONTROL

The video control circuitry (Figure 15) generates velocity proportional unblanking gates for the vector mode and selects appropriate unblanking pulses according to mode. It also supplies velocity magnitude data to the display driver and generates a recording strobe for x and y.

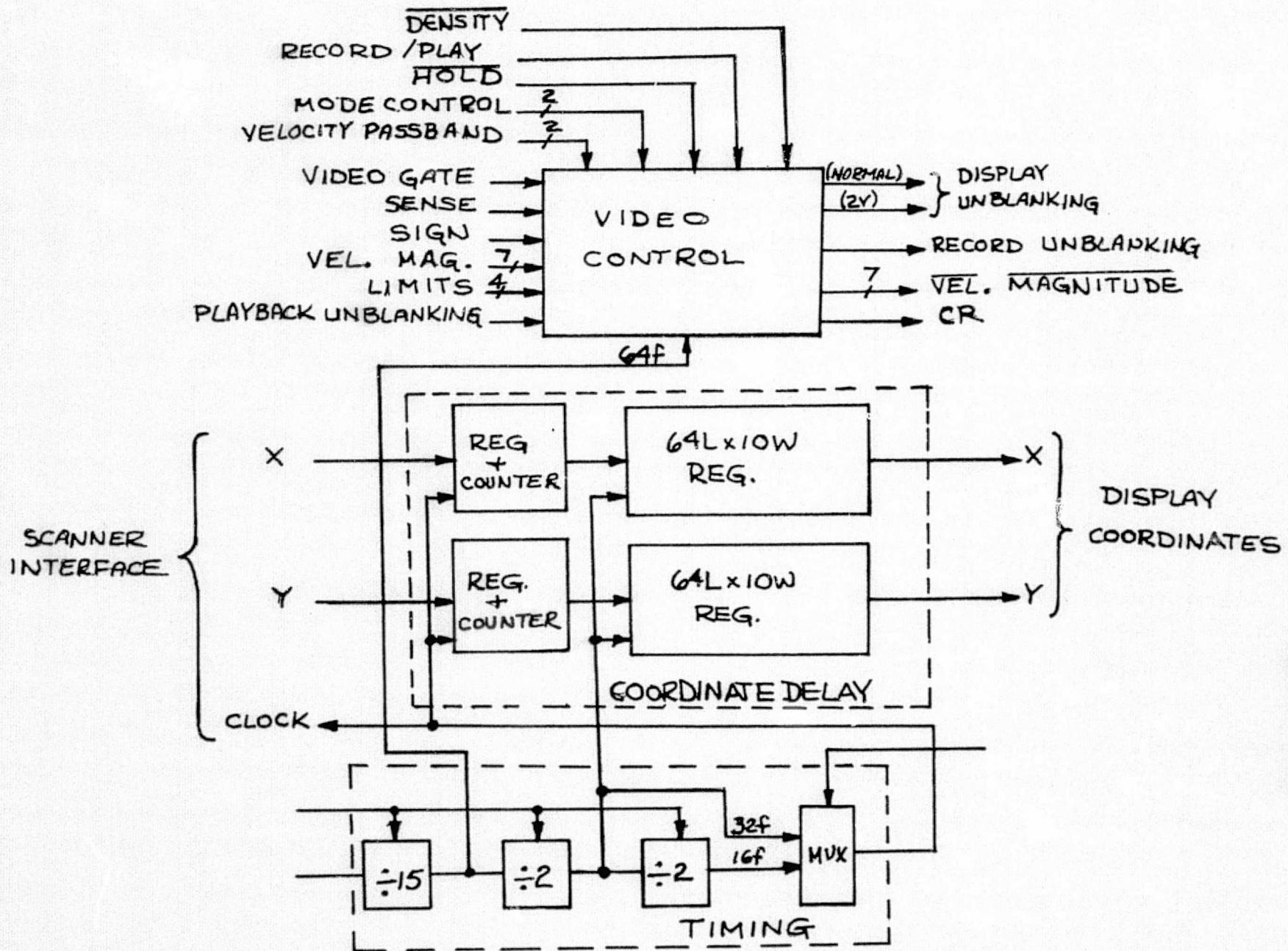


Figure 14. Display Buffer

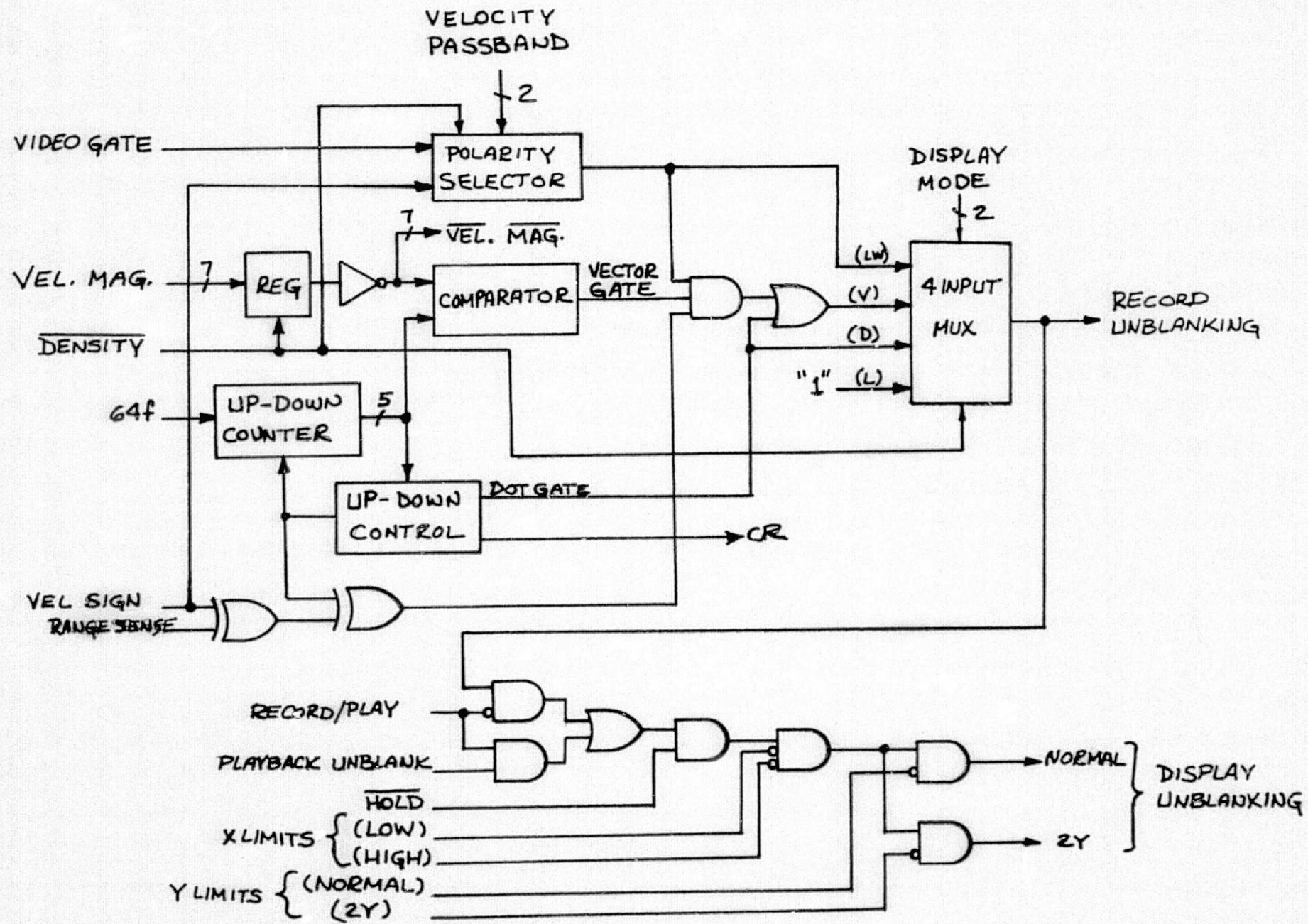


Figure 15. Video Control

The vector gate is generated by comparing the inverted velocity magnitude to the output of an up/down counter which is clocked at a rate of 64 counts per frame (64f). The counter counts up during the first half of the frame and down during the last half. Depending on the range sense* and velocity sign, the appropriate half (early or late) of the vector gate is chosen for unblanking. Typical operation for positive range sense with both velocity polarities displayed is shown in Figure 16. The up/down control circuit also generates a strobe (CR) to the formatter for storing digital x and y.

A four input multiplexer selects the proper unblanking signals according to mode. The video gate, the indicator that all the discriminator tests have been passed at some time during the frame, is passed through the polarity selector circuit which determines (from a front panel control) which polarities (plus, minus, or both) are to be displayed. This selector output determines unblanking in the line width mode and gates unblanking in the vector mode. In the dot mode, only the dots themselves are unblanked; the entire scan (within the display limits) is unblanked in the line mode. In all modes, the display is blanked whenever either co-ordinate exceeds either of its display limits. The display is also blanked whenever the front panel hold switch is actuated.

In the density mode of velocity discrimination, the display mode reverts to line width modulation, the modulation (i. e., velocity) is set to zero, and the velocity passband is set for both polarities at all times.

TIMING

Timing circuits to generate the 64f and 32f clocks and the clock for the scanner co-ordinates are included on the buffer card. The 64f clock is generated by dividing the rate of a 960 counts/frame clock (BPC) by 15; the 32f clock is obtained by dividing the 64f rate by two.

The 32f clock is sent to the scanner in all integration times except 0.5 msec. For this shortest integration time, the display resolution is limited by the display tube itself, and the scanner clock rate can be reduced by a factor of 2. This reduction results in a scanner clock rate of 16 cycles per integration period, or 32 kHz.

* This signal indicates the sign of the rate of range change.

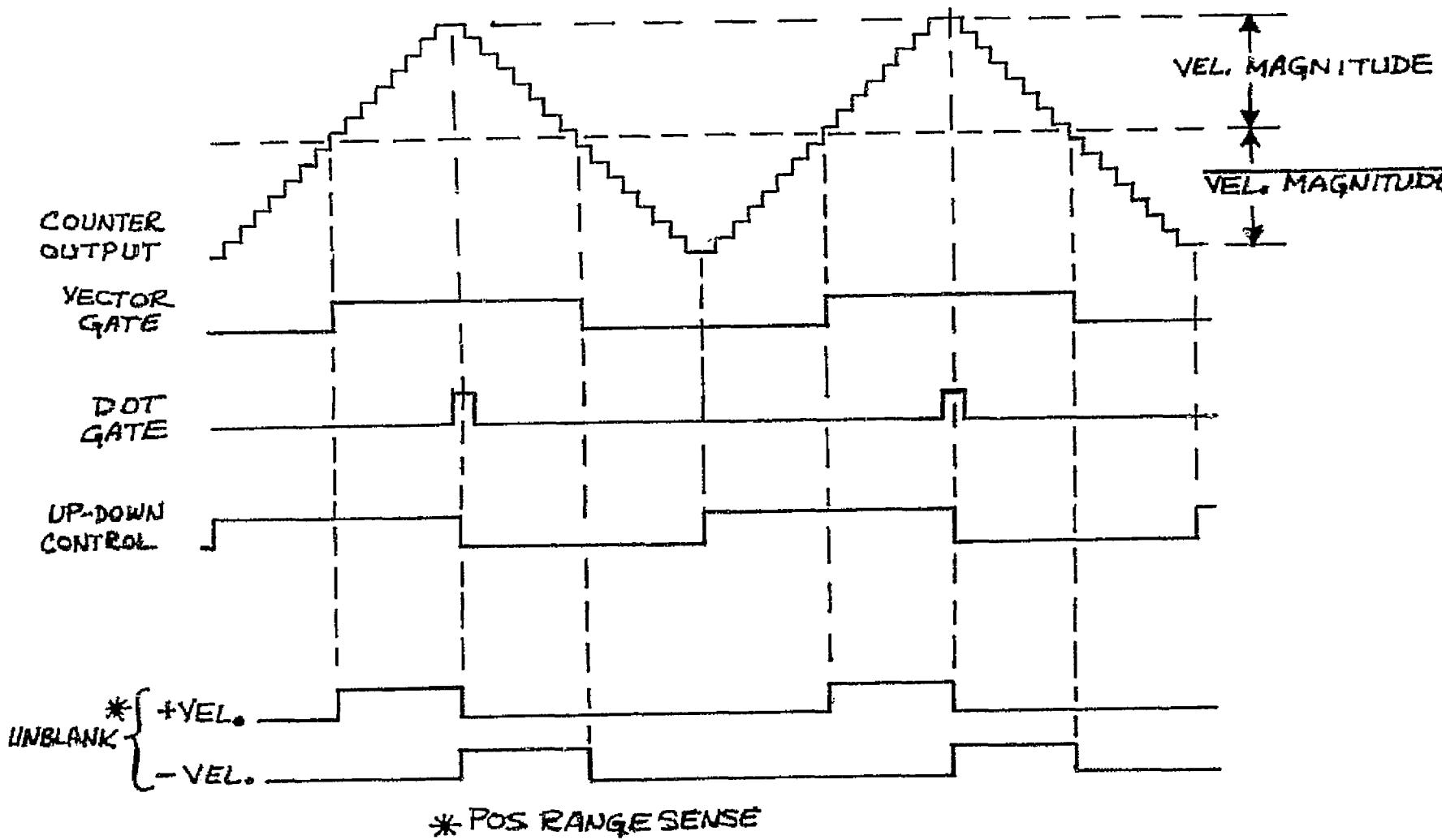


Figure 16. Vector Generation

CO-ORDINATE DELAY

The co-ordinate delay circuitry delays the x and y scanner co-ordinates by two integration periods. The delay is accomplished by clocking 64-bit long shift registers at 32 counts/frame (32f). To aid in testing the interface card, counter/registers are used for the first stage of the register. These circuits can be switched into a counting mode in which various rates of linear sweep of x and y can be produced for testing.

Listed in Table IV are requirements for the digital x and y inputs from the scanner. The display format places the point (x = 60m, y = 0m) at the lower left of the display. The co-ordinate x represents ground range and y represents altitude. The x and y data must be synchronized to the clock supplied by the processor. Set-up and hold times are with respect to the positive-going edge of the clock.

TABLE IV SCANNER CO-ORDINATES

Input Levels	TTL
Fan In	Two Standard Loads
Logic	Positive
Coding	Binary
Word Size	10 Bits
LSB	5/8 Meter
Coverage	0 to 640 Meters
Delay	< 1 Clock Cycle
Max. Clock Frequency	32 kHz
Clock Levels	TTL
Triggering	Positive Edge
Set-up Time	100 nsec
Hold Time	50 nsec

The co-ordinate word size chosen enables the 640 meter range to be covered in 0.64 meter steps, which is compatible with the 1.0 meter resolution of the display in the normal (x_1) scale factor. This register length and clock rate will not degrade the display resolution at the 1 msec integration time. Degradation of display resolution at various scan rates for longer integration times is shown in Figure 17.

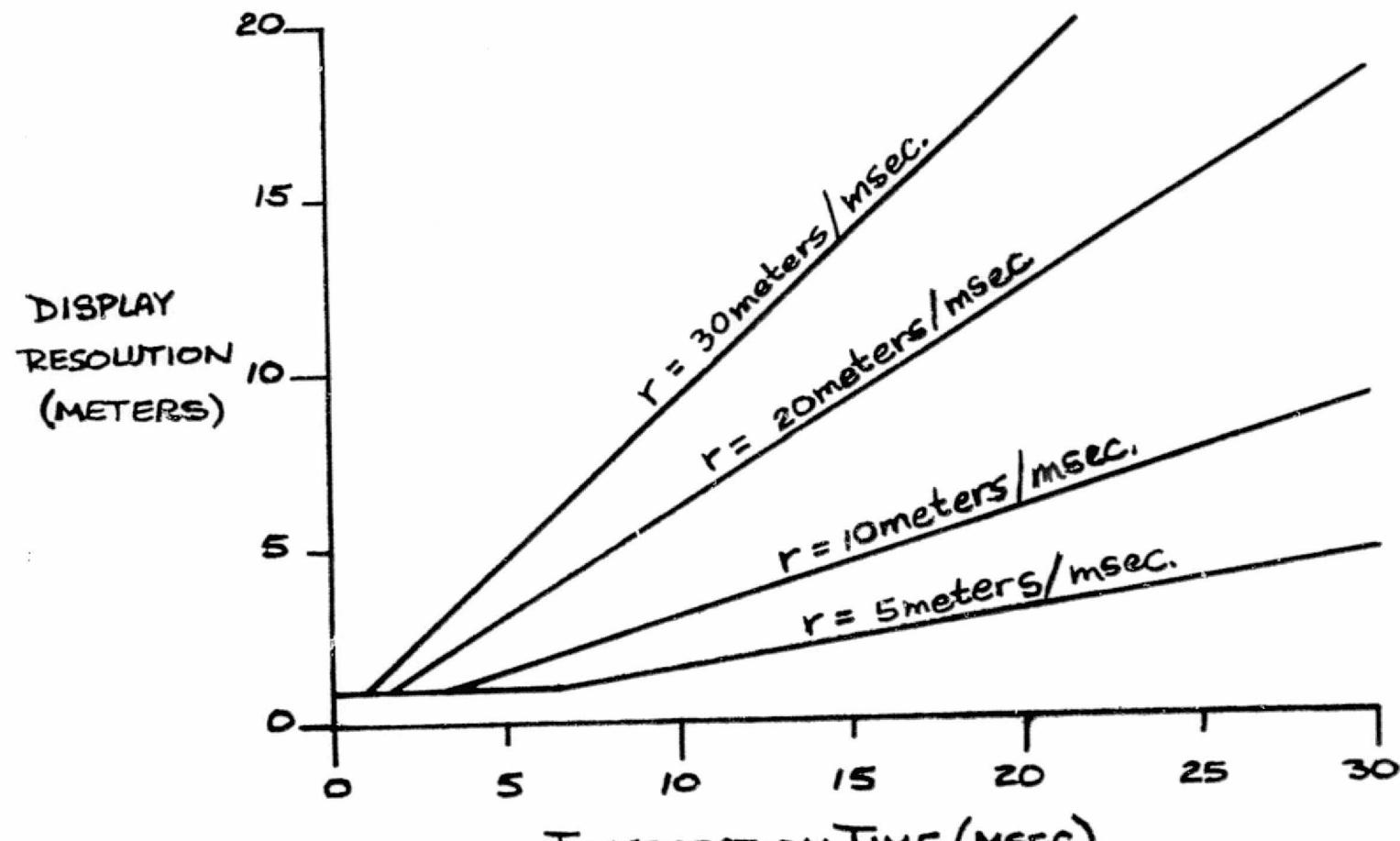
With the two expanded scale factors, the resolution is improved slightly because the resolution of the display tube ceases to be an important factor in overall resolution.

5.4.4 DISPLAY DRIVER CARD

The display driver converts the co-ordinates to analog, amplitude modulates them where appropriate, and scales them for display. Other functions performed by the card are selection of record or playback operation and generation of the x and y limit signals. Figure 18 is a block diagram of the card.

The Δx and Δy signals for width modulation are generated by $\pm 45^\circ$ phase shifts of an amplitude modulated sine wave. The modulating signal is the analog velocity for line width modulation or a fixed voltage for dots. An analog multiplexer is used for selection and gating of the modulating signal.

The digital co-ordinate inputs are summed with the Δx and Δy signals to produce x and y for analog recording. Relays K1 and K2 select record or playback co-ordinates for scaling and display. Scaling is accomplished by amplifiers with programmable gains. The limit signals are generated by comparing the display co-ordinates to fixed thresholds.



- r = SCAN RATE
- NORMAL SCALE FACTOR (540m x 405m DISPLAY)

Figure 17. Display Resolution

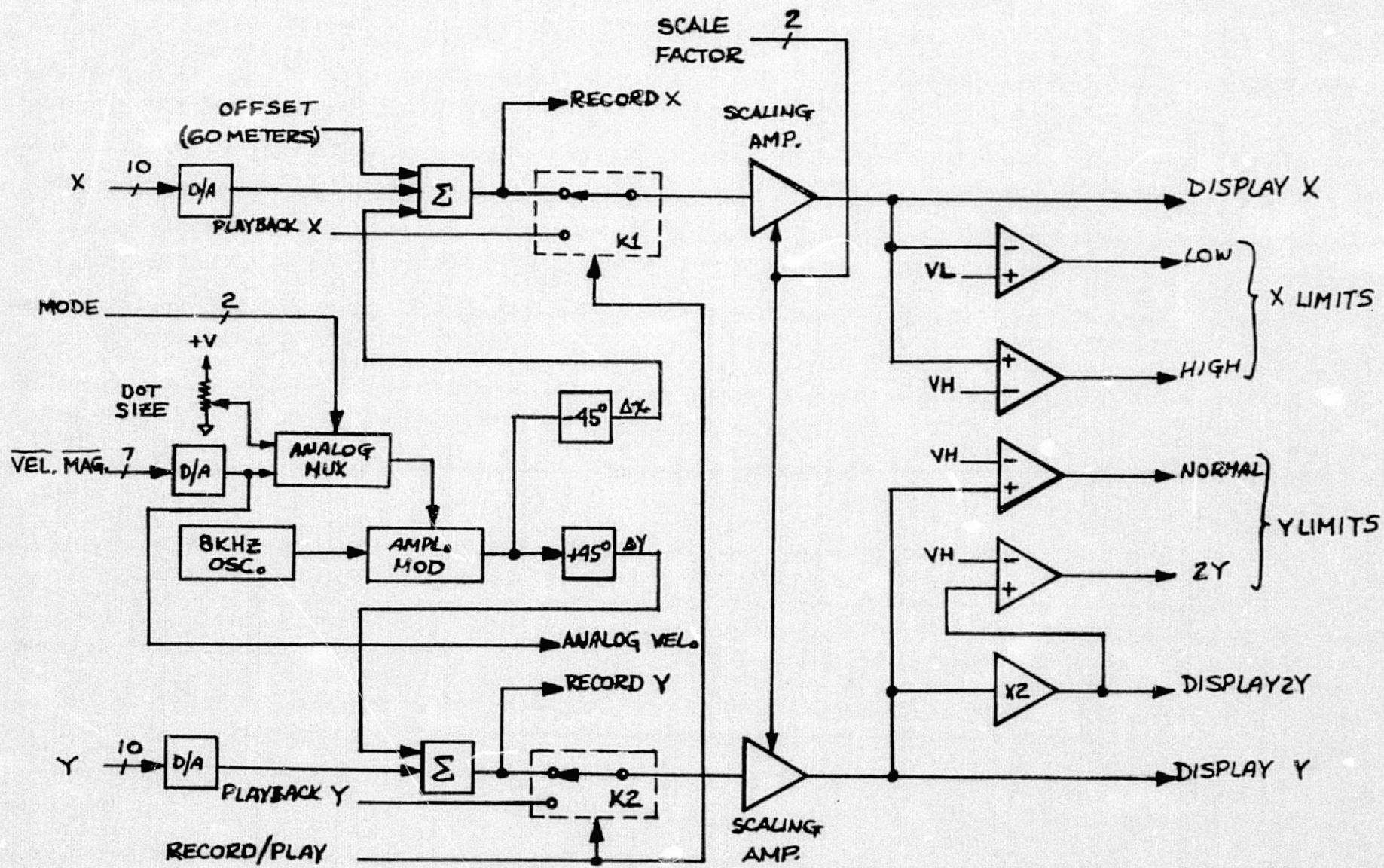


Figure 18. Display Driver



5.4.5 ANALOG RECORDING

Analog signals are available at the interface output which make playback directly from the Ampex CP-100 recorder to the display possible. The following signals are included:

<u>Designation</u>	<u>Signal</u>	<u>Level</u>	<u>Scaling</u>
XAR	Display X	-0.18 \leftrightarrow 1.74V	3mV/Meter
XAR	Display Y	0 \rightarrow + 2.56V	4mV/Meter
ZAR	Unblanking	0 \rightarrow + 2.0V	-
VAR	Analog Velocity	0 \rightarrow - 5.0V	39 mV/Cell

The display coordinate signals are large enough to make full use of the S/N potential of the recorder. Coordinate noise on playback will be about 2 meters rms at 7-1/2 ips and higher. Recording speeds below 7-1/2 ips are not recommended because the recorder bandwidth severely limits display resolution at lower speeds.

5.5 FORMATTER

The formatter is a single card which is intended to combine information from various portions of the system and to transform this information into an all-serial format for recording on one track of a wideband tape recorder. The spectrum integrator provides most of the information and timing signals required by the formatter.

Figure 19 is a block diagram showing how the formatter is organized, while Figure 19a portrays the timing relationships among the various signals for one integration period or frame time. During the gap, auxiliary data consisting of a 31 bit synchronization code, a four digit run number from front panel switches, a mode word, a frame count, and X and Y position words are converted to serial form in the multiplexer array. This signal drives the Bi- ϕ encoder which develops the output signal exemplified in Figure 19a. The mode word describes the specific configuration of the system regarding integration time, velocity coverage, linearity, and whether or not the translator is present. The frame counter has six BCD digits, increases its count by one at the start of each frame, and can be reset to zero by means of a front panel pushbutton. Additional logic determines when the counter has overflowed (after 8.334 minutes at a 0.5 millisecond integration time); this condition lights a front panel overflow indicator.

Following the gap, data from the integrator, already in the proper sequence, is simply converted to serial form and bi-phase encoded. Figure 11 shows the organization of the output sequence and the relationship between output word number N and doppler velocity for two different coverage modes. Output specifications are listed in Table V.

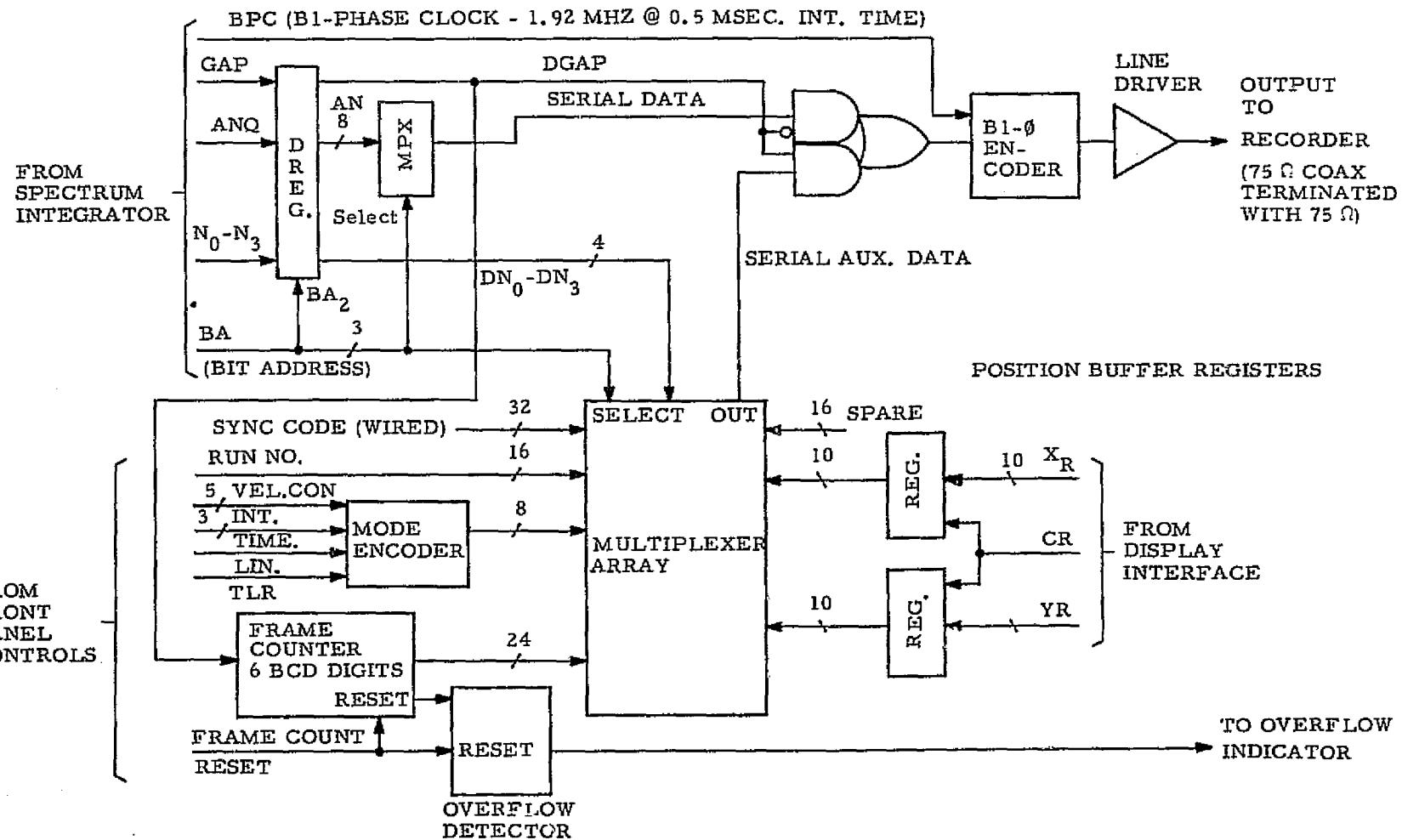


Figure 19 Formatter Block Diagram

RAYTHEON COMPANY

REGULATORY DIVISION



Figure 19a. Timing Diagram

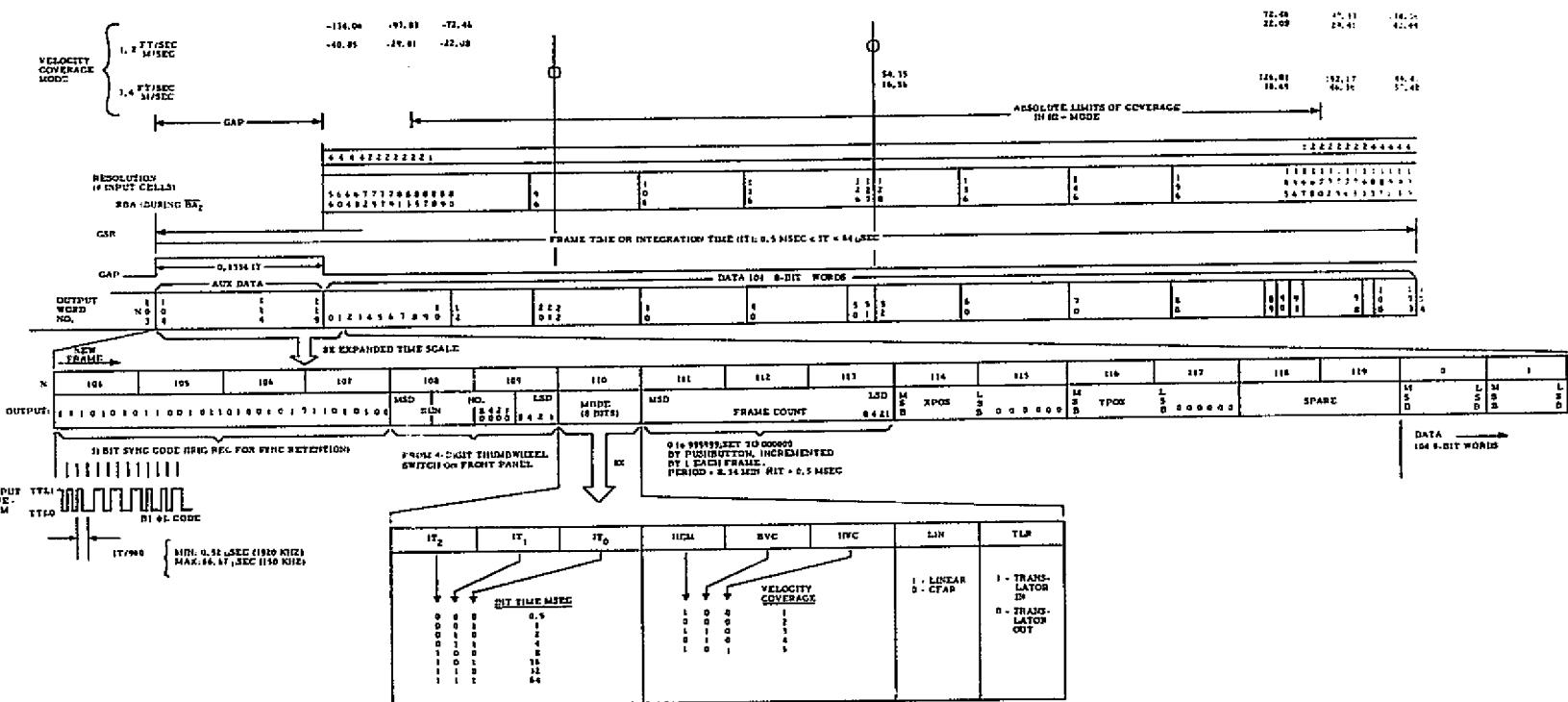


TABLE V
OUTPUT SPECIFICATIONS

No. of Outputs	1
Output Levels and Drive Capability	Standard TTL thru 75 Ω Coax (See Texas Instr. SN 74128 Data Sheet)
Frame Time (IT)	0.5, 1, 2, 4, 8, 16, 32, or 64 milliseconds
No. words per Frame	120
No. bits per Word	8
No. bits per Frame	960
Bit Time	0.52 to 66.67 μ sec (IT/960)
Bit Coding	Bi- ϕ L : "1" { TTL1- { TTL1- { TTL0- ; TTL0- { TTL0- { TTL0-

SECTION 6

OPERATIONAL CHECKS

The operational checks described here are intended to help in the setting of front panel controls and aid in demonstrating the Signal Processor is functioning properly. Some of the modes and controls are not covered due to lack of field operation and complexity involved to check these functions. A complete test is covered in the LVD performance.

6.1 POWER ON

Connect the Signal Processor to a 115 Vac $\pm 5\%$ power source. Turn on the front panel power on switch and check for the following voltages.

+15 Vdc ± 0.2 Vdc
-15 Vdc ± 0.2 Vdc
+5 Vdc ± 0.1 Vdc
-5 Vdc ± 0.1 Vdc
+24 Vdc ± 0.3 Vdc
+120 Vdc ± 6.0 Vdc

6.2 SPECTRUM ANALYZER

Set the front panel controls as follows.

Input Level	- 0 (Minimum)
AGC Threshold	- 10 (Maximum) with AGC disabled and G-2 set for +2.32 Vdc
AGC Time Constant	- Long
Linearity	- Linear
Velocity Coverage	- To desired coverage
Integration Time MSEC	- To desired integration time
Input Signal Mode	- To desired mode corresponding to velocity coverage

Connect an oscilloscope with a frequency resolution of 100 MHz (454A or equivalent) to the front panel Spectrum Analyzer Output (J14). Trigger the oscilloscope from the front panel CRO trigger (J15). Connect the input signal cable to the desired input (Non-translated-Translated) making sure the signal

never exceeds 100 millivolts into 50 ohms (-7 dBm). Observing the oscilloscope with approximately 6 MHz of bandwidth and 0.1 volt per division of signal adjust the input level so there is approximately 0.15 volts peak of wind doppler giving approximately 10 dB range for the vortex doppler signal. (With a maximum doppler signal input of -7 dBm the doppler signal at the Spectrum Analyzer output should be 0.5 volt peak.) See Figure 20.

6.3 SIGNAL INTEGRATION AND VELOCITY DISCRIMINATION

Set the front panel controls as follows.

Amplitude Threshold	- 000
Velocity Threshold	- 00
Width Integration Number of Cells	- 1
Density Threshold	- 00
Velocity Descriminator Mode	- Width Integration

Connect an oscilloscope to the integrated output test point (J31) on the rear panel of the Signal Processor. Trigger the oscilloscope from the GAP test point (J32). Viewing the oscilloscope, adjust the velocity threshold thumb wheel until the wind signal is blanked (approximately 1.8 ft/sec per thumb wheel digit), see Figures 21 and 22. Set the Amplitude threshold for an acceptable level blanking the noise floor as seen on the oscilloscope (see Figures 21 and 22).

6.4 DISPLAY

Set the front panel controls as follows.

Display Mode	- Test 2
Scale	- 1
Velocity Passband	- +
Normal/Playback	- Normal
Normal/Hold	- Normal

Connect the Tektronix 613 display scope to the rear panel normal display connector (J18). Provide scanner interface signals for a display width (X) of 195 meters (X-10 bit word 291) and a display height (Y) of 101.25 meters (Y-10 bit word 190). Adjust the Velocity and Amplitude threshold to zero. This should give a dot (wind doppler signal) in the positions indicated.

<u>Scale Position</u>	<u>X position from left edge</u>	<u>Y position from bottom</u>
1	5 cm	3.75 cm
2	10 cm	7.5 cm
3	15 cm	11.25 cm

Place the Normal/Hold switch in the hold position; the 613 display should blank. By returning the switch to normal the display should unblank. Place the mode switch in the following positions with the Velocity and Amplitude thresholds at zero and the Scanner interface scanning in a normal operating mode.

Display 1 - A line segment on the display with the width proportional to the velocity of the signals for that period.

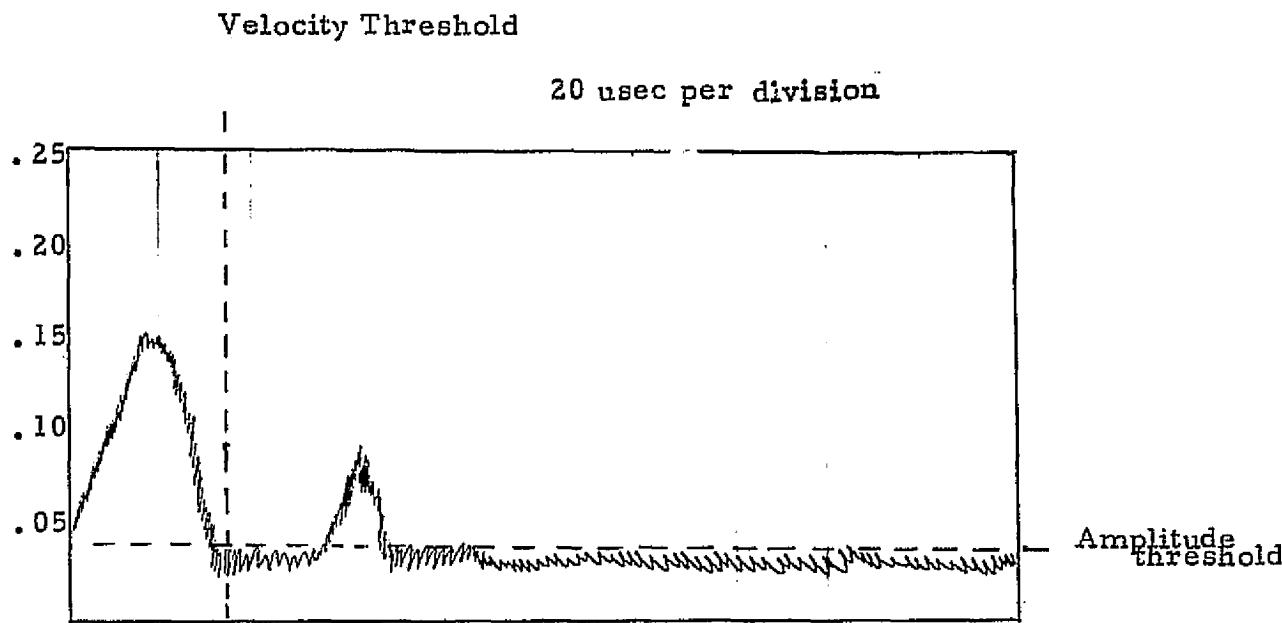
Display 2 - A dot display with the half inside the dot designate velocities toward the laser and the half outside the dot would designate velocities away from the laser.

Test 1 - A line segment unblanked at all times tracing the entire scan on the display.

Test 2 A dot display only unblanked during the center of each integration period.

6.5 FORMATTER FRAME COUNTER

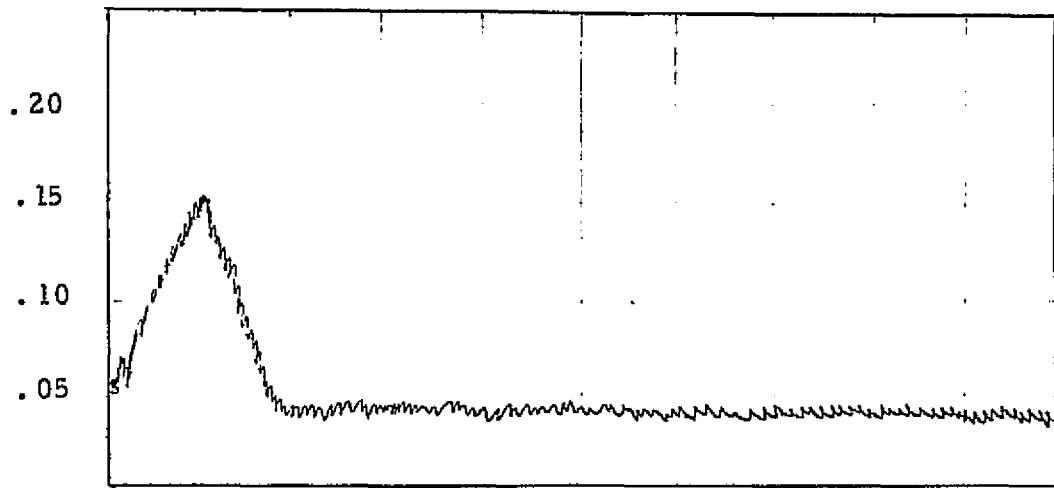
Place the Integration Time MSEC switch in the 0.5 MSEC position. Reset the frame counter. The overflow lamp should come on in 8.334 minutes.



Example: From Flight Test of LVD System Conducted at MSFC, 12 December 1973.

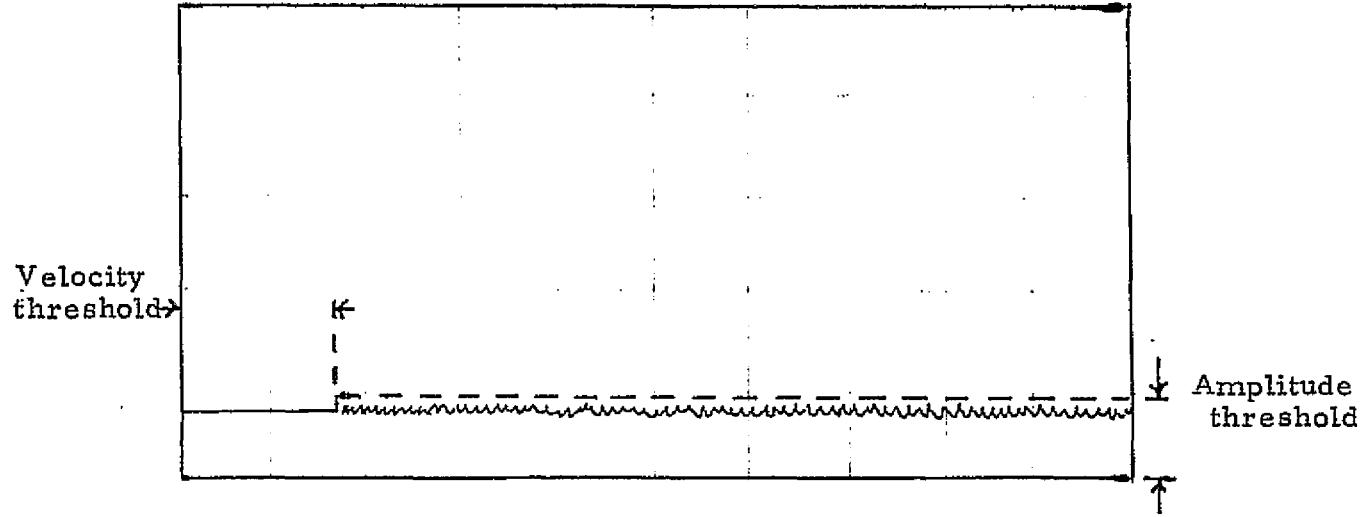
Wind Signal Ranged up to Approximately 700 KHz at .16 Volts Amplitude.
Spectral Return from Expected Vortices Ranged About 1.5 MHz at .095
Volts Amplitude. System Noise About .03 Volts. Velocity Threshold
set to 15 (900 KHz). Amplitude Threshold Set to Blank the System Noise.

Figure 20. Example: Wind Signal Spectrum Analyzer Output



Example: Width Integration and Amplitude threshold outputs with wind signal and system noise. Velocity threshold and Amplitude thresholds set to zero.

Figure 21. Width Integration and Amplitude Threshold Outputs (Zero)



Example: Width Integrator and Amplitude threshold output. Velocity and Amplitude thresholds set to blank unwanted wind and system noise doppler data.

Figure 22. Width Integration and Amplitude Threshold Outputs (Proper Level)

SECTION 7

PERFORMANCE TESTS

The tests described here are intended to demonstrate the ability of the LVD signal processor to meet the performance requirements.

Although the tests, as listed below, are identified in terms of the characteristics called out by the statement of work, they are configured to prove out all performance specifications given.

List of tests:

- a. Velocity Coverage
- b. Velocity Resolution
- c. Dynamic Range
- d. CFAR Mode
- e. A/D Conversion
- f. Integration Time
- g. Width Integration
- h. Velocity Threshold
- i. Amplitude Threshold
- j. Density Mode
- k. Display Interface
- l. Scanner Interface
- m. Analog Recorder Interface
- n. Formatter

7.1 VELOCITY COVERAGE

7.1.1 TEST DESCRIPTION

The purpose of this test is to demonstrate the capability of the signal processor to perform processing of signals over frequency ranges corresponding to at least the following velocity ranges:

Without translator	0 to ± 170 ft/sec
With translator	-100 to ± 100 ft/sec

The low-velocity coverage is required to extend to with 100 kHz of the frequency corresponding to zero-doppler.

7.1.2 TEST PROCEDURE

The velocity coverage capability is to be demonstrated for the ranges given above, plus the additional velocity range cited in the design plan, by connecting a conventional CW signal generator to the appropriate input (non-translated or translated) of the signal processor and tuning the signal generator through a range while observing the signal processor response. The signal processor response can be observed at several points. The analog output directly from the spectrum analyzer can be viewed at the jack provided on the front panel of the signal processor (J14). An equivalent digital output can be obtained by using the "test card" to provide the width integrator output from the velocity discriminator. In this case the "width integration number of cells" control is set to "1".

As the signal generator frequency is varied over a range, a point will be reached where the amplitude of the signal processor output will drop down due to the filter characteristics within the spectrum analyzer. The frequency points where the amplitude is reduced by 3 dB are the nominal limits of the velocity coverage.

7.2 VELOCITY RESOLUTION

7.2.1 TEST DESCRIPTION

This test will demonstrate the ability of the signal processor to resolve input signals as a function of their frequency distribution. The resolution required is as given in Figure 2.

The overall resolution obtained is dependent on both the spectrum analyzer and the spectrum integrator. The spectrum analyzer portion determines the intrinsic resolution available, in that the overall resolution can never be better than that obtained in this part. The integrator, because of its sampling action in the analog-to-digital conversion process, can effectively reduce the resolution by sampling less frequently the analyzer output. The resolutions given in the figure referred to above are intended as the overall resolution expected.

7.2.2 TEST PROCEDURE

The test uses the same signal processor configuration to view the response of the processor as for the velocity coverage test. The two tests should therefore be performed at the same time. The only difference is that two cw signal generators are used instead of one. The signal levels from the two generators are arranged so as to always be equal at the input to the signal processor input as the frequency separation between them and the amplitude of the input signals is varied. The frequency of each generator is monitored with an electronic counter.

By observing the processor analog output (after the spectrum analyzer) or the digital output (width integrator output, with the number of cells set to one), the frequency separation for which two distinct outputs are seen is noted. The same determination is made over a range of input signal levels equal to the dynamic range (35 dB for the linear operating mode).

7.3 DYNAMIC RANGE

7.3.1 TEST DESCRIPTION

The dynamic range test determines the maximum amplitude range of multiple-input signals over which an unambiguous measurement of input velocity is obtained. The circuit characteristics which determine the useful dynamic range available are such things as harmonic distortion in video amplifiers, spurious product generation in mixers, and the sidelobes produced by the pulse compression action of the spectrum analyzer.

This test is primarily aimed at the linear operating mode, for which a dynamic range of 35 dB is specified. For the CFAR mode, the dynamic range is less, depending on the bandwidth being analyzed. The procedure is the same in any case.

The test arrangement is similar to that for velocity resolution and should therefore be performed in conjunction with this test.

7.3.2 TEST PROCEDURE

Signal generator are used to apply a single signal, and then two simultaneous signals, to the processor input. The processor response is viewed in

the same manner as for the velocity coverage test. For a single input signal, the signal level is set to the maximum input level (nominally 100 millivolts) with the AGC disabled ("AGC Threshold" set to maximum level) and the "input level" control set to its normal position (to be determined). The frequency of the signal generator is then varied over a range corresponding to the velocity coverage range of the processor and the output response observed. Throughout the velocity coverage range, there should be no other peaks in the output response besides the main response which are less than 35 dB below the main response. The 35 dB-down level is determined by reducing the input level of the signal generator by 35 dB when it is centered in the velocity coverage band.

A similar test is made with the two signal generators, each providing an input level of 70 millivolts to the processor. In this case, only the "non-translated" input to the processor is used and the signal generators are maintained at a frequency separation of roughly one megahertz as they are both tuned through the low-velocity coverage region. The output response is observed to determine that there are no spurious responses generated which are not at a level exceeding the 35 dB-down level determined in the single-signal case.

7.4 CFAR MODE

7.4.1 TEST DESCRIPTION

This demonstrates the ability of the signal processor to produce a signal output response having spectrum analyzer, spectrum integrator and velocity discriminator performance characteristics while maintaining the background noise level constant at the output of the velocity discriminator.

7.4.2 TEST PROCEDURE

The test is performed by connecting a single signal generator to the input of the signal processor, along with a noise source, and observing the output in the same manner as for the velocity coverage test while tuning the signal generator frequency throughout the velocity coverage ranges. The noise source should be capable of producing noise across the velocity coverage band which is 10 to 20 dB greater than the normal background noise as viewed at the spectrum analyzer analog output jack when in the linear mode.

Differences which are normal for the CFAR mode as compared to the linear mode are:

- a. The dynamic range will be less and will depend on the velocity band being spectrum-analyzer. For the 6 MHz band used in the high-efficiency modes, the dynamic range will be approximately 17 dB. Also, the dynamic range is measured as the ratio of the response amplitude produced by a single-frequency input signal with the noise source turned off, to the amplitude produced by noise alone.
- b. For two simultaneous cw signal generator inputs, more than two output responses can be obtained. However, the output response having the highest amplitude will always correspond to the frequency of the input signal having the greater input level.

7.5 A/D CONVERSION

7.5.1 TEST DESCRIPTION

All circuitry on the A/D Converter Card (A3) is tested by following procedures outlined in this section. An analog ramp is used to exercise all levels of the converter and to verify its 8-bit resolution capability. Clock frequency and power supply voltages are critical to proper A/D converter as well as overall system operation; checks on them are therefore needed before proceeding with the ramp test. A simple test of the signal detector is included.

7.5.2 TEST EQUIPMENT REQUIRED

- a. Analog waveform generator capable of generating a linear ramp ranging from -4 to +4 volts in about 250 μ s and of being triggered by a TTL logic-level transition, e.g., EH 139B.
- b. RF signal generator capable of +5 dB \pm 1 dB output into 50Ω at 60 MHz.
- c. Frequency counter capable of frequency measurements to 6 MHz.
- d. Oscilloscope with variable delayed sweep.
- e. Special TEST CARD supplied by Raytheon.

7.5.3 TEST PROCEDURE

7.5.3.1 Power Supply Test

Check power supply voltages with all cards in place and verify that they are within the following ranges:

+15V ± 0.2 V

-15V ± 0.2 V

+5V ± 0.1 V

-5V ± 0.1 V

If any voltage is out of tolerance, correct it by adjusting the appropriate power supply. DO NOT ALTER THE OVERRANGE VOLTAGE TRIP LEVEL ADJUSTMENTS. Remove the ACCUMULATOR CARD (A4) and the INTEGRATOR OUTPUT CARD (A5) and recheck the +5V power supply voltage.

7.5.3.2 Clock Frequency Test

a. On the A/D Converter Card (A3), disconnect the signal detector output from the sample-and-hold unit input. Set up the ramp generator to apply the waveform described above to this input. Insert the TEST CARD in place of A4, connect its trigger output to the ramp generator, and observe its analog output on the scope.

b. After a minimum of 15 minutes for warm-up, observe the staircase ramp in detail. Verify that all 256 levels are present and that the waveform is monotonic. If necessary, adjust the pedestal offset control (R3) to obtain the best waveform.

7.5.3.4 Detector Test

a. With no rf at the detector input, adjust the COARSE OFFSET control, R1, until the detector output is about +3.9 volts.

b. Apply a +5 dBm ± 1 dB, 60 MHz CW signal to the 50Ω detector input and adjust the GAIN control, R4, to bring the output to about -3.8 volts.

c. Connect the detector output to the sample-and-hold unit input. With zero signal at the detector input, adjust the fine and coarse bias controls (R2 and R1) until the A/D output code alternates between 00000000 and 00000001.

d. Apply the +5 dBm signal to the input again. Adjust the BIAS control, R4, until the output code alternates between 1111111 and 1111110.

7.6 INTEGRATION TIME

7.6.1 TEST DESCRIPTION

Two test options are provided:

a. WITHOUT A/D CONVERTER - All circuitry on the ACCUMULATOR (A4) and INTEGRATOR OUTPUT (A5) cards, as well as the clock, timing waveform generator, and output register of the A/D CONVERTER CARD is tested. The A/D output register is configured as a counter, reset to zero at the center of each spectrum analyzer cycle, by adding two temporary jumpers. The resulting test spectrum is useful in evaluating the performance of all circuitry on A4 and A5 at all integration times between 0.5 and 64 milliseconds.

b. WITH A/D CONVERTER - Everything mentioned above plus the sample-and-hold unit, the buffer, and the A/D converter on the A/D CONVERTER CARD (A3) is tested. Any arbitrary waveform can be set up to simulate time-invariant spectra for the purpose of testing, not only the integrator, but also following circuitry such as the velocity discriminator. The pulse generator simulates the spectrum analyzer and detector in this test.

7.6.2 EQUIPMENT REQUIRED

a. WITHOUT A/D CONVERTER

1. Special TEST CARD supplied by Raytheon.
2. Oscilloscope with variable delayed sweep (e.g., Tektronix 454A).

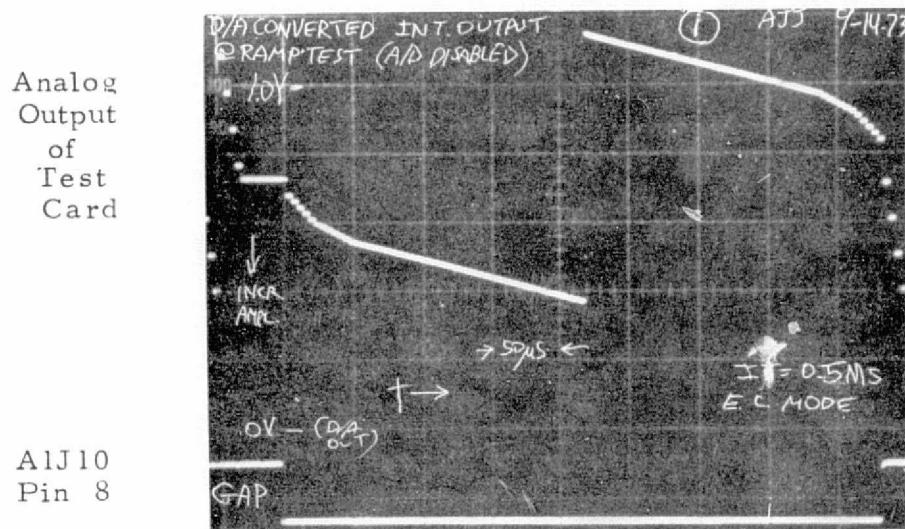
b. WITH A/D CONVERTER

1. Special TEST CARD supplied by Raytheon.
2. Oscilloscope with variable delayed sweep (e.g., Tektronix 454A).
3. PULSE GENERATOR with double pulse output, variable interpulse delay, independent width adjustments, variable rise and fall times, and trigger input (e.g., Chronetics PG-33).

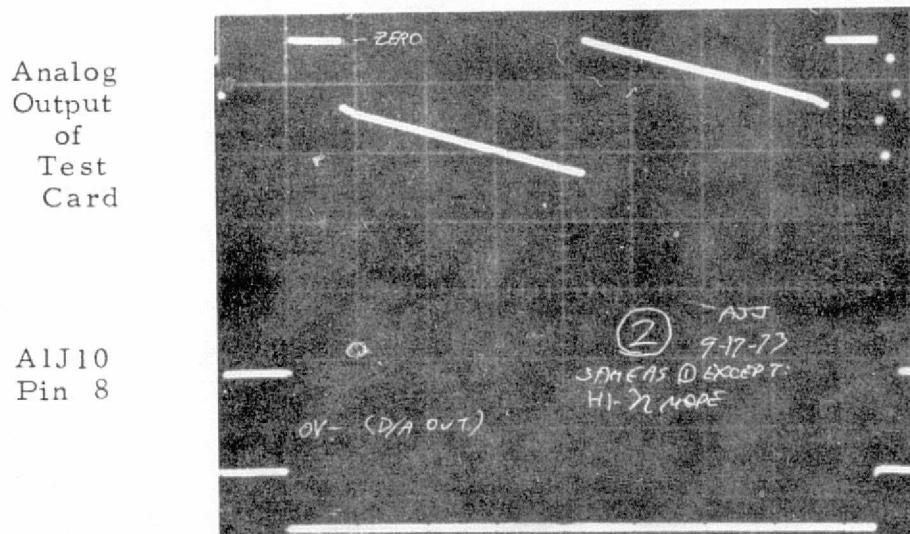
7.6.3 TEST PROCEDURE

7.6.3.1 Test Without A/D Converter

Apply the appropriate jumpers to the A/D converter card (A3). Remove the FORMATTER and VELOCITY DISCRIMINATOR cards (A5 and A6) and insert the TEST CARD in A5. Switch the Velocity Coverage control to position 2. Observe the waveforms shown in (a) of Figure 23.



(a) Velocity Coverages 2 and 4



(b) Velocity Coverages 1, 3, and 5

Figure 23. Integrator Output Converted to Analog

Switch the integration time control to each position and verify that the period of the waveform, as in the figure, is equal to the integration time selected. Amplitudes should not vary with integration time. Repeat the preceding test with the velocity coverage switch set at 4; the results should be the same.

Select a 0.5 ms integration time and verify that the waveforms shown in (b) are obtained with velocity coverages 1, 3 and 5.

Remote integration time selection can be demonstrated by switching the integration time control to "remote", grounding the appropriate pins on A1J20, and comparing the resulting period of the waveforms in the figure with that specified in Table II .

7.6.3.2 Test with A/D Converter

Remove jumpers from A3 and connect the output of the double pulse generator to the input of the sample-and-hold unit, and SAT (test point on A5) to the pulse generator trigger input. The integrated output can be observed using the test card as was done above, or it can be used to test other portions of the system.

7.7 WIDTH INTEGRATION (VELOCITY DISCRIMINATOR)

7.7.1 TEST DESCRIPTION

This test demonstrates the width integration capability of the velocity discriminator. The width integrator takes a running average of the sum of the amplitudes in a number of contiguous velocity cells (Q) selected by the front panel switch.

A cw input to the spectrum analyzer is employed to approximate an impulse in the velocity domain. The output of the width integrator is approximately equal to its impulse response; for this type of "moving window" integrator, the impulse response is a pulse as wide as the window (Q cells). The effect of varying Q on the width integrator output is illustrated in Figure 24.

7.7.2 TEST PROCEDURE

Apply a cw signal to the spectrum analyzer input and display the output of the width integrator on an oscilloscope using the test card. Turn the width

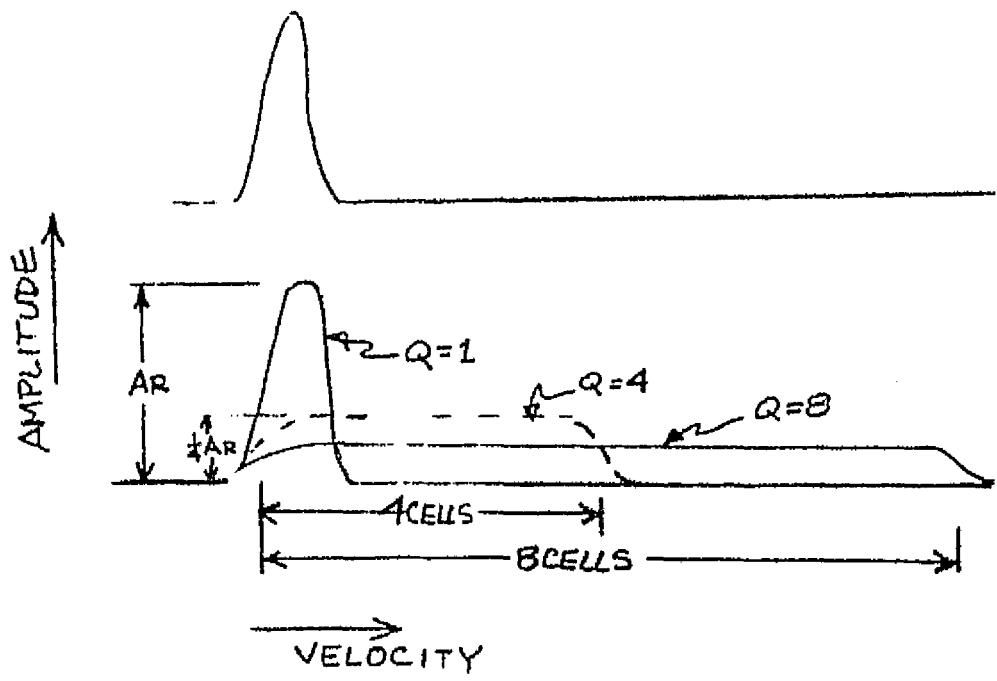


Figure 24 Width Integrator Impulse Response

integration (Q) selector to 1 cell integrated. Apply the input frequency for minimum output pulselwidth. By varying the input amplitude or the vertical scale factor of the oscilloscope, set the peak output amplitude to a fixed number of divisions. This amplitude is the output reference amplitude (A_R).

Turn the width integration switch through each of its positions and observe the output pulse. For values of Q which are powers of two, the output pulse amplitude is A_R/Q . For values of Q which are not powers of two, the output amplitude is $1.5A_R/Q$. The width of the output is Q cells for all values of Q.

7.8 VELOCITY THRESHOLD (VELOCITY DISCRIMINATOR)

7.8.1 TEST DESCRIPTION

This test demonstrates the capability of the velocity discriminator to gate out a band of velocities near zero. A substantial level of noise is used as the spectrum analyzer input, so that all the input velocity bins have signal present. The velocity discriminator rejects a band $\pm N_o$ cells wide around the zero velocity bin, where N_o is the setting of the velocity threshold. This rejection band is illustrated in Figure 25.

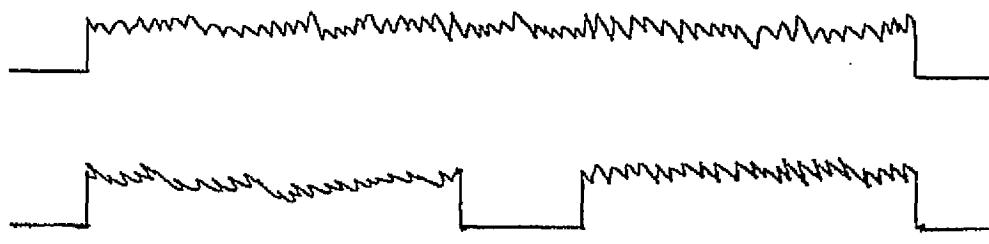


Figure 25. Velocity Threshold Effect

7.8.2 TEST PROCEDURE

Display the width integrator output on an oscilloscope using the test card. Set the width integration to one cell. Apply wideband noise level to the input of the spectrum analyzer sufficient for a meanwidth integrator mean output of about 1/4 full scale. To aid in measuring the mean output, use a high a value of spectrum integration time.

As N_o (the velocity threshold) is increased, a $2N_o$ cell wide notch appears in the width integrator output. The amplitude during the notch is zero.

7.9 AMPLITUDE THRESHOLD (VELOCITY DISCRIMINATOR)

7.9.1 TEST DESCRIPTION

This test demonstrates the amplitude threshold capability of the velocity discriminator. The input to the analyzer is two cw signals of different amplitude and frequency. Since the velocity discriminator examines the velocity cells serially, a second signal cannot be peak detected if it has been preceded by a higher amplitude, lower frequency signal. For this reason, the lower amplitude signal is placed at a lower frequency than the higher amplitude signal.

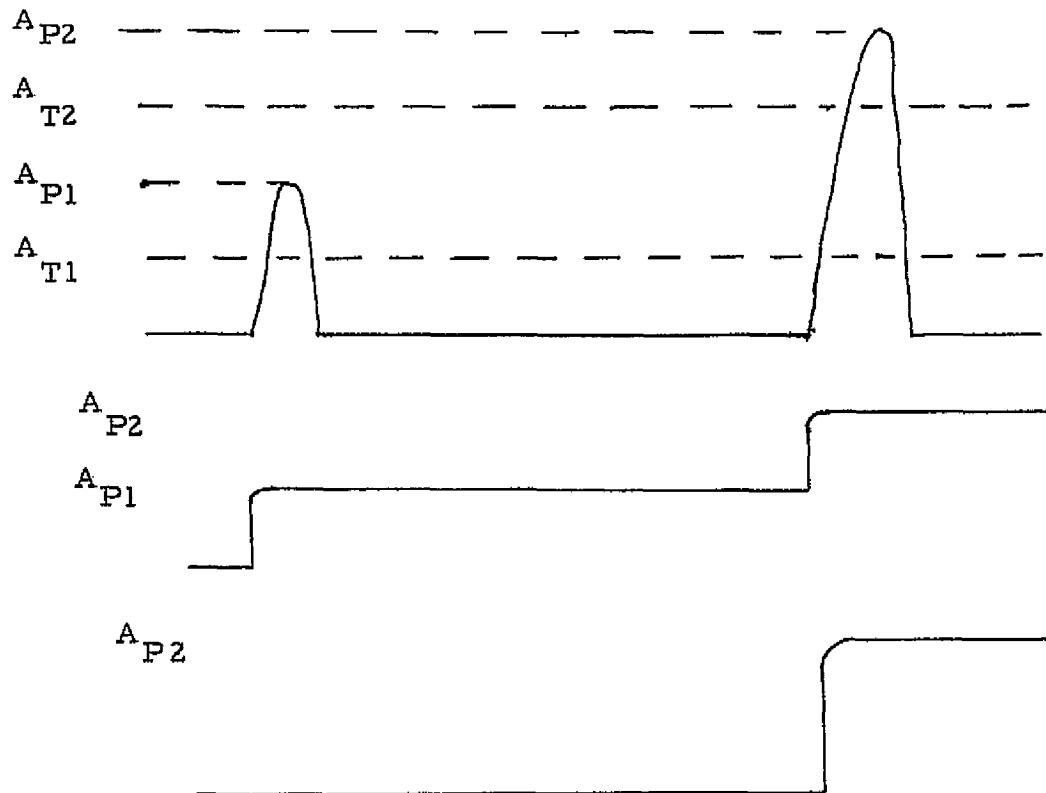


Figure 26 Amplitude Threshold

Figure 26 above illustrates the effect of the amplitude threshold on the peak detected output for two threshold levels. When threshold A_{T1} - which is below both spectral peaks - is applied, both peaks (A_{P1} and A_{P2}) are detected. By applying threshold A_{T2} such that $A_{P1} < A_{T2} < A_{P2}$, the detection of the first peak (A_{P1}) is eliminated, and only A_{P2} is detected.

7.9.2 TEST PROCEDURE

Set the width integration selector to one cell and display the width integrator output on an oscilloscope using the test card. Apply the sum of two cw signals to the analyzer input and adjust the frequencies of the signals for about a 20-cell separation between the two spectral peaks. Insure that the output amplitude peaks are below 1/8 of full scale.

Place the unit in the width integration mode. Set the amplitude threshold at 50 and increase the level of the lower frequency input until the spectral peak is barely peak detected. Set the amplitude threshold at 100 and increase the level of the higher frequency input until the second spectral peak is barely peak detected.

With the input levels set as described, amplitude threshold below 50 result in both signals being peak detected. Amplitude threshold between 50 and 100 result in detection of only the higher frequency peak. The peak detector has no output when the threshold is raised above 100.

7.10 DENSITY MODE (VELOCITY DISCRIMINATOR)

7.10.1 TEST DESCRIPTION

In the density mode of operation, the velocity discriminator does not employ width integration or detection of the highest spectral amplitude. The discriminator instead counts the number of cells in which the amplitude and velocity threshold are exceeded. Because of the specialized nature of this mode, generation of a signal with a spectrum adequate for making definite measurements of discriminator operation is very difficult. Therefore, a simulated spectrum, with a well defined number of cells above the thresholds, is applied to the spectrum integrator input.

7.10.2 TEST PROCEDURE

Place the velocity discriminator in the density mode with a density threshold of ten cells, a velocity threshold of zero cells, and an amplitude threshold of 32 cells. Display the width integrator output on one oscilloscope trace using the test card, and the video gate* on the other trace.

Connect a pulse generator to the input of the spectrum integrator. Trigger the generator from the spectrum integrator. Rise and fall times of the generator pulse should be as small as possible. Set the generator output level for a 1/4 full scale width integrator output pulse.

Set the generator pulse width for a narrow (one or two cells) width integrator output pulse. The video gate should be low at this time.

*This signal is a one-bit indicator that a sufficient signal has been detected by the discriminator.

Slowly increase the generator pulselwidth until the video gate goes high. The width integrator output pulse should be 10 cells wide at this time.

Repeat the procedure above for several density threshold values. The width of the output pulse (in number of cells) at the time when the video gate goes high should be equal to the density threshold in all cases.

7.11 DISPLAY INTERFACE

7.11.1 TEST DESCRIPTION

The following group of tests demonstrate the capability of the display interface to drive the Tektronix 613 display. The features demonstrated are operation in the four display modes, multiple scale factor selection, hold capability, and velocity passband selection. These features are described in detail in the display interface design plan.

A single set-up procedure (7.11.2.1) is used for all four test sections. If this procedure is followed, any of the three test sections can be performed individually without performing the entire test.

Coordinate positions (x, y) referred to in the tests are in cm, with (0, 0) at the lower left of the display.

7.11.2 TEST PROCEDURE

7.11.2.1 Setup

Remove A40 of the display interface card and plug in the test module. Manually reset the test counters. The interface card now generates test ramps for x and y internally. These ramps are identical, so that a line at a 45° angle is generated on the display. The y intercept of the line is 60 meters.

Unblanking and width modulation of the line are a function of front panel settings and input signals. In particular, the two operating modes require the presence of a digital velocity at the input of the interface. For the purposes of these tests, any input spectrum (at the analyzer input) or simulated spectrum (at the A/D converter) with a single peak which can be moved over the entire range of velocity cells is sufficient.

7.11.2.2 Modes

Place the display in a test mode 1 and the scale factor in position 1. A line from (0, 2.2) to 12.8, 15) appears on the display. Placing the display in test mode 2 produces a row of dots 1.5 cm apart along the same line.

Place the display in display mode 1 and vary the velocity over its range. The line now has a width proportional to the magnitude of the velocity. Placing the display in display mode 2 and varying the velocity over its range produces vectors with length proportional to the log of the velocity magnitude.

7.11.2.3 Passband Selection

With the display in display mode 2 and a positive velocity, move the passband selector through its three positions. The vector is blanked only in the negative passband position. Change the velocity to negative and move the passband selector through its positions again. The vector is blanked only in the positive passband position.

7.11.2.4 Scale Factor

Place the display in test mode 1 and move the scale factor factor switch through its positions*. This procedure stores three parallel lines with 45° slopes on the display. The y intercepts of the lines are 2.2 cm, 3.3 cm, and 6.7 cm.

Erase the display and return the display scale factor to 1. Store the normal scale factor line on the display and then turn down the display intensity. Switch the display connector to the 2Y connector on the rear panel and increase the intensity until a second line is stored. The slope and y-intercept of this second line should be double that of the normal line.

7.11.2.5 Hold Capability

Place the display in test mode 1 and depress the hold switch. The display is blanked by depression of the switch.

* It is helpful to turn down the display intensity during scale factor changes.

7.12 SCANNER INTERFACE

7.12.1 TEST DESCRIPTION

This test checks the correspondence of the digital scanner coordinate inputs with position on the display. A check of the scanner clock is also included.

7.12.2 TEST PROCEDURE

The display should be set in "test mode 1" with normal scale factor (position 1).

Apply the two sets of x and y input words listed below. The displayed spot in each case should be in the position listed.

Input Words				Scanner Position		Display			
x	MSB	LSB	y	MSB	LSB	Range (m)	Height (m)	x(cm)	y(cm)
1000011111			0111100000			351	288	13.0	10.7
0111100000			1000011111			288	351	10.7	13.0

The scanner clock can be checked with an oscilloscope. In the 1/2 ms integration time, its period is $31.25 \mu s$. For all other integration times, its period is 1.64 of the integration time. The rise and fall times of the clock should be less than 100 ns, and the symmetry should be approximately 50/50. The minimum amplitude is 2.4V into 75 ohms.

7.13 ANALOG RECORDER INTERFACE

7.13.1 RECORDING

This test is a check on the analog recorder outputs of the display interface. To perform the check, follow the setup procedure of Section 7.11.2.1 and place the display in display mode 2. Ramps of the full-scale amplitudes listed below are present on x and y. The Z output is a vector gate with a width that can be varied by varying the velocity. The velocity output is a dc level which varies linearly with velocity magnitude.

Recording Output Levels

<u>Designation</u>	<u>Signal</u>	<u>Level</u>
XAR	Display X	- .18 → 1.74V
YAR	Display Y	0 → +2.56V
ZAR	Unblanking	0 → +2.0 V
VAR	Analog Velocity	0 → +5.0 V

7.13.2 PLAYBACK

This test checks playback operation by use of the test signals described in the previous section. To apply the test signals for playback operation, connect the x and y record outputs to their respective playback inputs and connect the playback Z input to the vector test point on the display buffer card.

Follow the procedure of Section 7.11.2.1, place the display in display mode 2, and depress the playback switch. A magnified (twice normal size) vector display is produced, demonstrating the increased sensitivity of x and y in playback.

7.14 FORMATTER

7.14.1 TEST DESCRIPTION

Data originating in various parts of the signal processor are shown to appear in the proper order in the all-serial digital recorder output. Data is first verified to be correct at certain test points on the FORMATTER card, A6, then the encoded output at AJ23 is compared with the test point waveform.

7.14.2 TEST EQUIPMENT REQUIRED

Oscilloscope with variable delayed sweep (e.g., Tektronix 454A).

7.14.3 TEST PROCEDURE

7.14.3.1 General

The following circuit cards must be in place for this test: A3, 4, 5, 6, and 8. The following test points are provided on the FORMATTER CARD, A6, to simplify time-location of data:

- a. DGAP is high during the gap when all auxiliary data is to appear. (Use this output to trigger the scope.)
- b. BA2 is a clock which has a period equal to that of eight output bits.
- c. DATA + AUXDATA is the data signal observed just prior to the biphase encoder (Logic 1 = HIGH). Unless specified otherwise, keep integration time control set at 0.5 ms.

7.14.3.2 Auxiliary Data Test

The 31-bit synchronization code should appear at DATA + AUXDATA and begin immediately at the low-to-high transition of DGAP. Verify that the code is correct. Next is a single zero followed by the RUN NUMBER code. Switch the run number thumbwheels on the front panel and observe the correct response in the data stream.

The 8-bit mode word is next; by switching the integration time selector, the velocity coverage switch, the linearity switch, and the input signal mode switch to each of their positions, verify that the correct code is obtained. Note that when the integration time is changed, the scope time base must also be varied because the output data rate is a function of integration time.

The 24 bits following the mode word are the frame count words which should be observed to be counting. Depress the frame counter reset button and note that all 24 bits go to zero. After releasing this button, wait about 8.32 minutes¹ at which time the frame counter overflow indicator will light. While waiting, verify that all 24 bits are counting.

The X and Y position words follow the frame count and can be tested by grounding the appropriate pins on the scanner interface connector, A1J17, while observing the data stream. X and Y are 10 bits each, with a 6-bit gap between them. Twenty-two bits after the LSB of Y, the DGAP signal should go to zero, beginning the data portion of the cycle.

¹Be sure to select a 0.5 ms integration time.

7.14.3.3 Data Test

Connect appropriate jumpers to the A/D CONVERTER (A3) to configure its output register as a counter. Observe the first 8-bit word after the high-to-low transition of DGAP. With velocity coverage 1, this word should be 00000000, with velocity coverage 2, it should be 01110110 (118). Ensure that all of the other words contain data. The numbers should increase with time until, near the mid-point of the data interval, they should drop to zero and then continue increasing with time.

7.14.3.4 Bi-Phase Output Test

Compare the waveform at A1J3 with that at the DATA + AUXDATA test point. When the test point is high, the output should be high during the first half of the bit time and low during the second. The opposite should be true when the test point is low.

Section 8. Processor Modifications

This section describes modifications made to the processor to improve dynamic range and provide four additional analog outputs.

DYNAMIC RANGE IMPROVEMENT

In order to make the spectrum integrator output quantization smaller, a piecewise linear approximation of a log converter has been inserted between the accumulator output and the I/O input. This converter compresses twelve bits into eight. Figures 27 and 28 are plots of the converter characteristic. With this modification, the processor output and amplitude threshold scaling are approximately 6 dB per 32 lbs.

ANALOG OUTPUTS

Four analog outputs have been added to the processor. Circuitry to determine values and convert to analog signals contained on the display driver card. Figure 29 is a typical spectrum output waveform illustrating the added outputs defined below.

- 1) Spectrum Output - The amplitudes (serially of all the cells over the velocity threshold, after width integration. This output leads the other analog outputs by one frame.
- 2) I_{PK} - The highest amplitude in a frame which is higher than the amplitude and velocity thresholds (V_T & I_T).
- 3) V_{PK} - The magnitude of highest velocity in a frame for which the amplitude threshold (I_T) is exceeded.
- 4) N_T - The total number of cells over the amplitude threshold in a frame.

Output levels are listed in Table VI.

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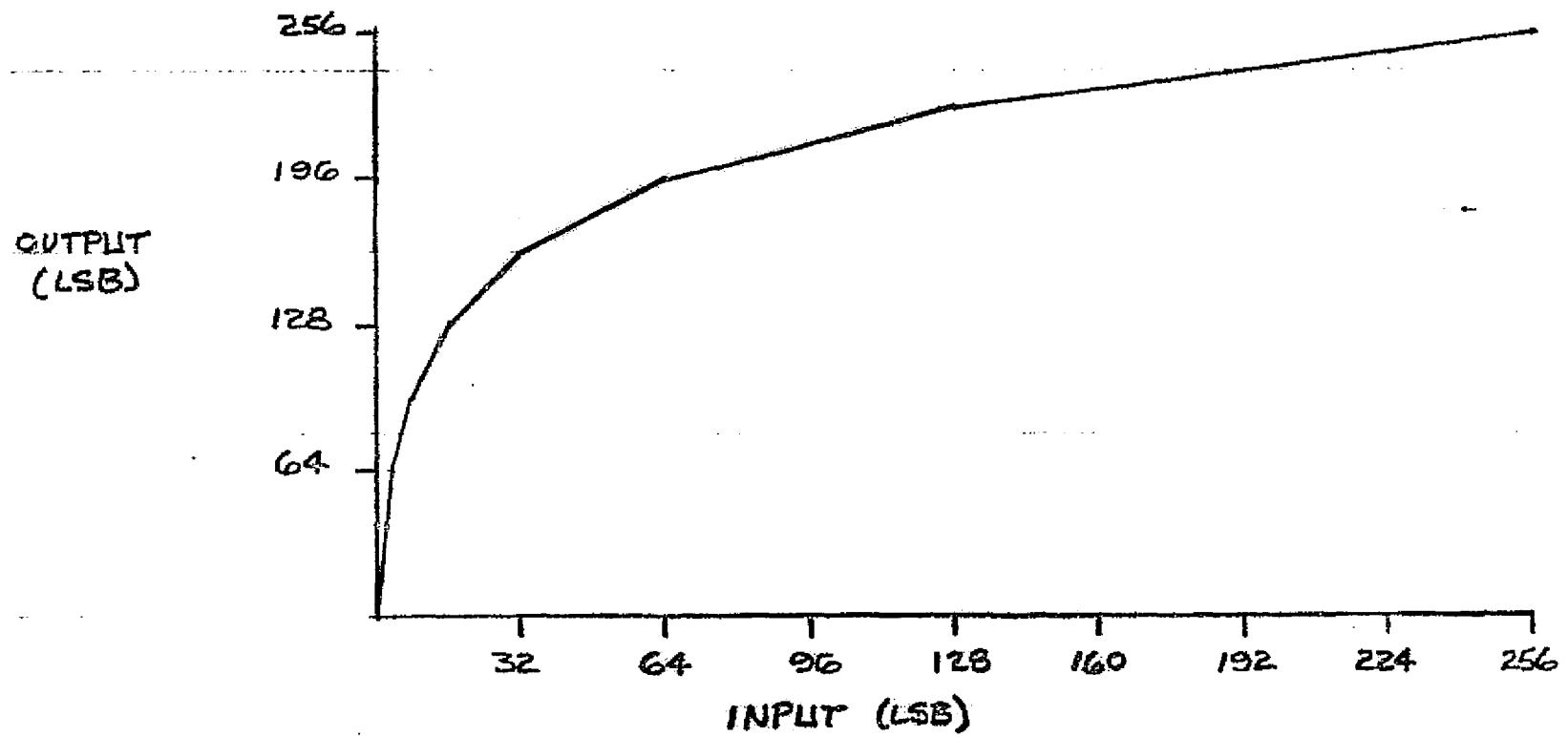


Figure 27. Log Converter Characteristic

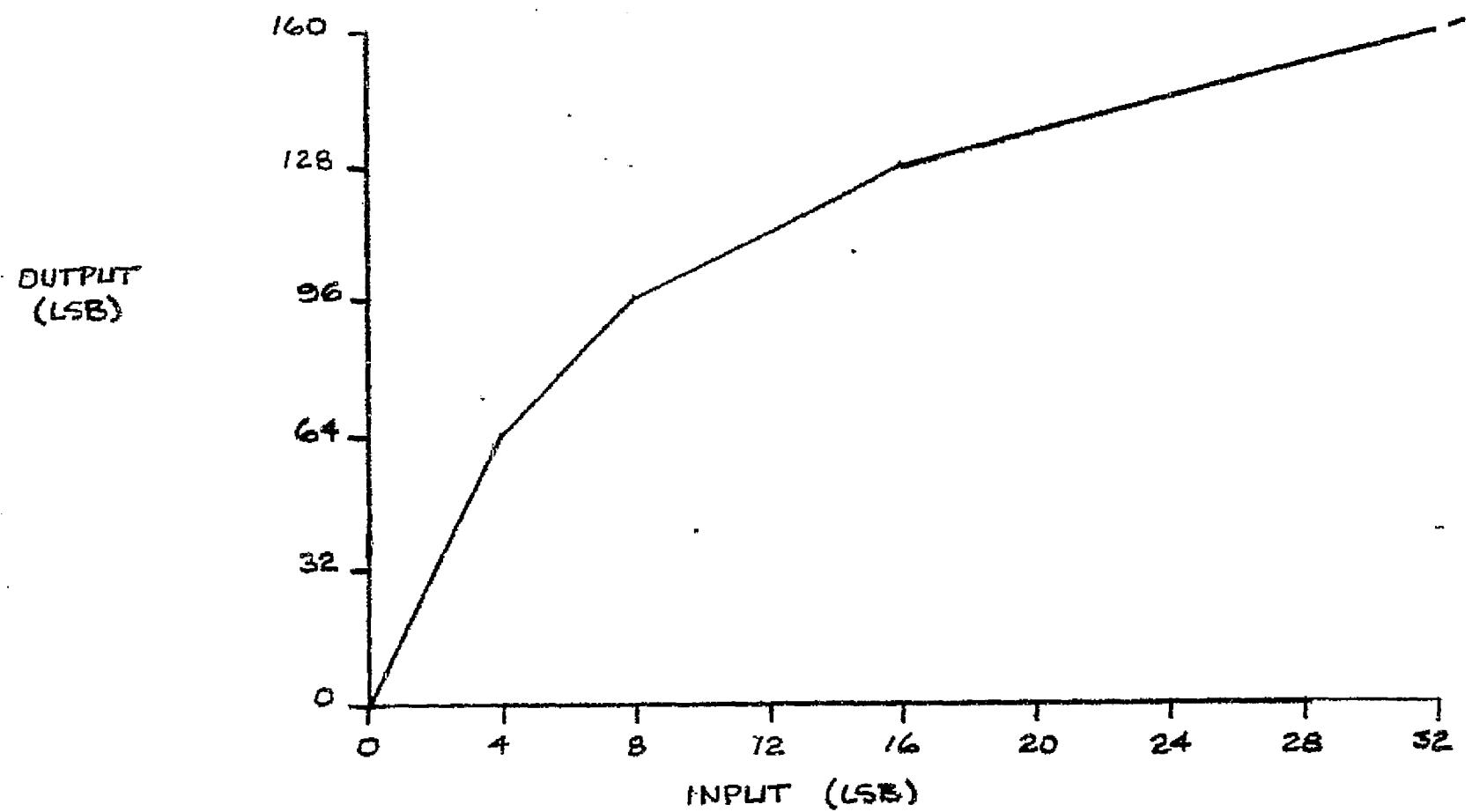


Figure 28. Log Converter Characteristic

Analog Spectrum Output
Spectrum Before Velocity Filtering
 $N_T = N_1 + N_2$

8-4

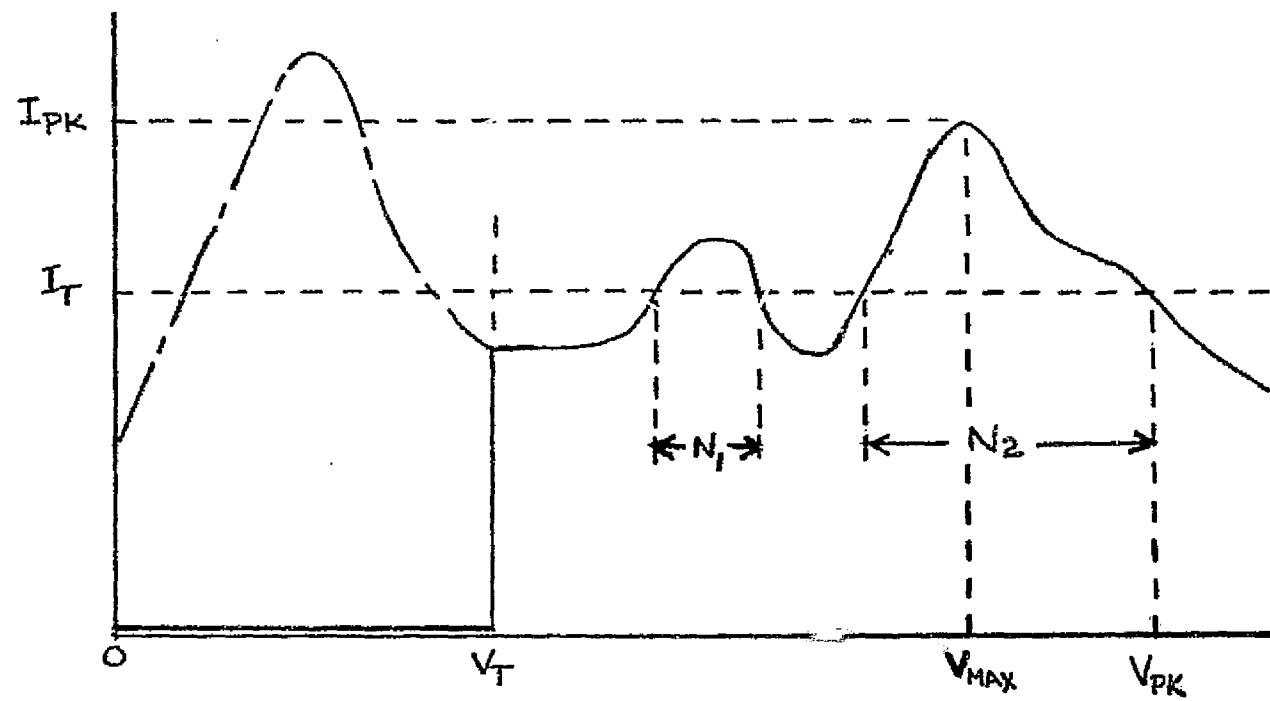


Figure 29. Spectrum Output

Table VI. Analog Output Levels

<u>Des.</u>	<u>Offset</u>	<u>Scale Factor</u>	<u>Max. Output</u>
Spectrum	0V	+. 15625V/dB	+7.5V
I_{PK}	-9.96V	+. 15625V/dB	-2.5V
V_{PK}	-9.96V	+. 078125V/Cell*	-3.71V
N_T	-9.96V	+. 078125V/Cell*	-1.91V
$V_{max.}$	0V	-. 0390625V/Cell*	-3.125V

*1 Cell = 104.17 kHz

APPENDIX A

IMPLEMENTATION OF IF FILTER BANKS
USING DISPERSIVE DELAY LINES

I. Description of Technique

The basic technique, as illustrated in Figure 1, is to generate a sine wave whose frequency is a linear function of time (chirp) and mix this with the signal to be analyzed. The output of the mixer is then applied to a dispersive delay line which has a linear delay versus frequency characteristic matched to the chirp pulse. The delay line acts to compress the input chirp pulse into a short pulse whose position in time is proportional to the input frequency, thus realizing a filter bank analyzer.

Figure 2 gives more detail on the waveforms in the system. Waveforms are shown for a single chirp pulse at the output of the variable frequency oscillator. The chirp pulse has duration T_c and its frequency is varied linearly from f_1 to f_2 . The frequency variation B_c is defined to be the difference between f_2 and f_1 . A fundamental quantity in the analysis is the dimensionless quantity $T_c B_c$, the time bandwidth product. In general it can be shown that the spectrum of the chirp pulse is approximately rectangular with bandwidth B_c , and the approximation improves as the time bandwidth product increases. When the chirp pulse is mixed with an input sine wave of frequency f_o , the only effect is to shift the frequency of the chirp pulse by f_o . Assuming that the upper sideband is utilized, the input to the dispersive delay line has a frequency excursion from $(f_1 + f_o)$ to $(f_2 + f_o)$.

The dispersive delay line must have a delay (time) versus frequency characteristic that is inverse to that of the chirp pulse in order to realize a matched filter. For instance, the frequency $(f_1 + f_o)$ is applied to the delay line at time $t = 0$, so that this frequency must be delayed by T_c seconds more than the frequency $(f_2 + f_o)$ which occurs at the end of the pulse. This gives the delay versus frequency characteristic of the surface wave delay line as shown in (c).

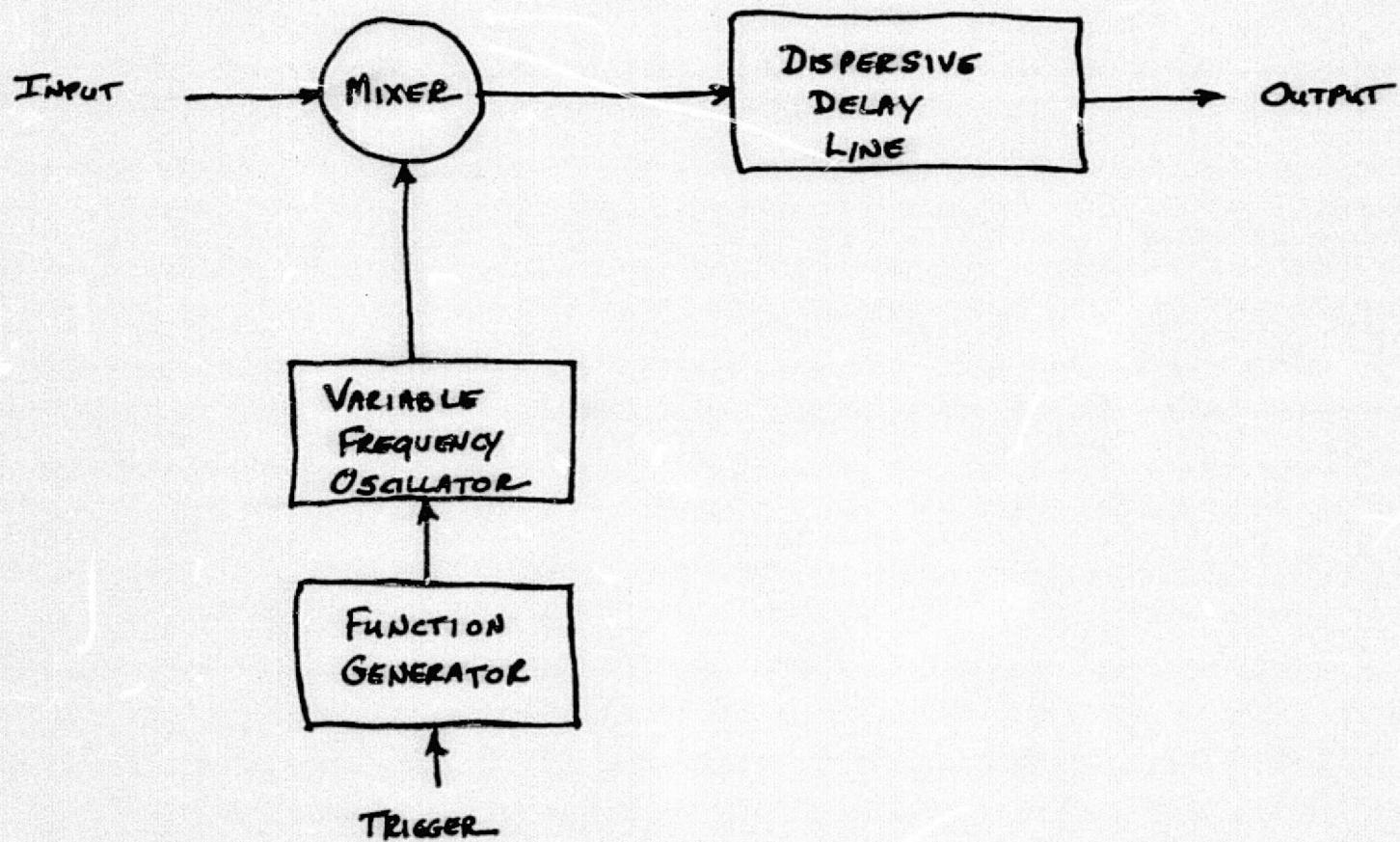
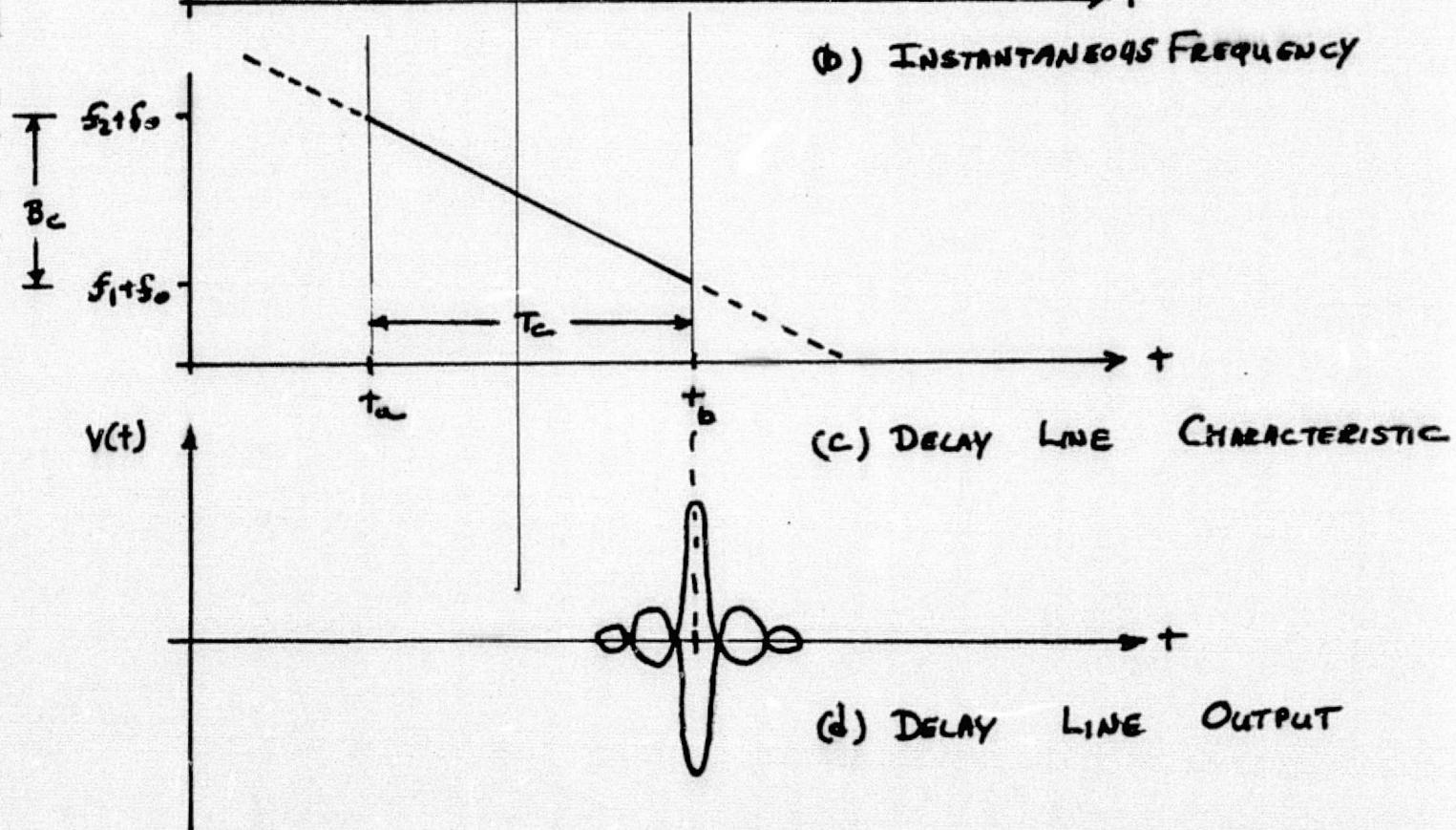
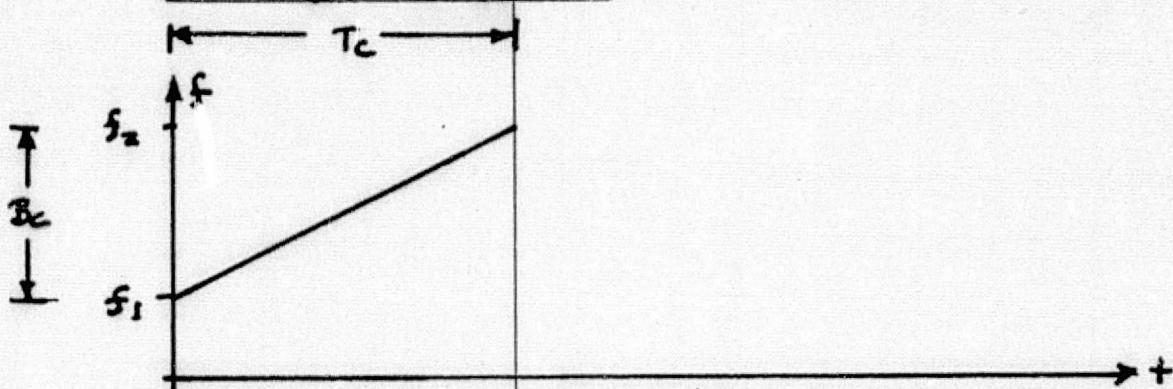
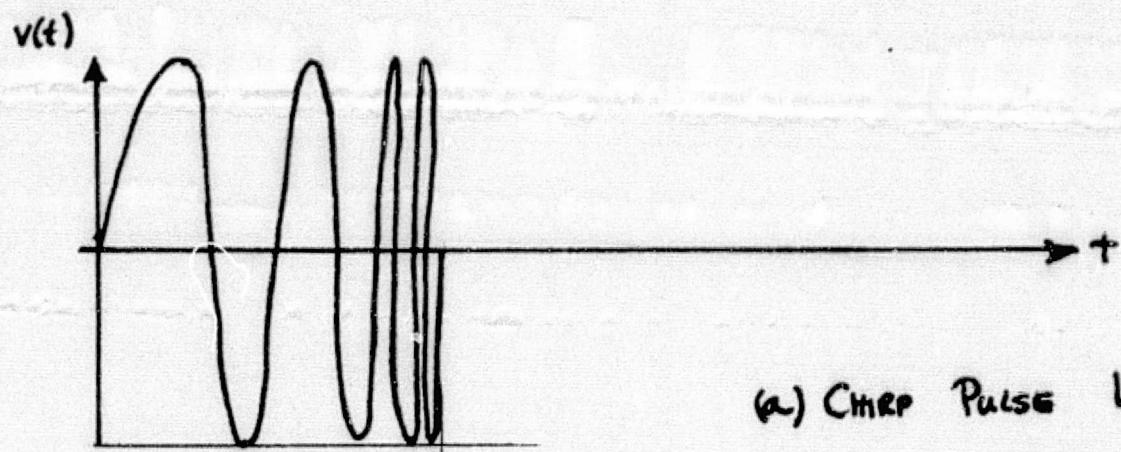


FIGURE 2. FILTER BANK IMPLEMENTATION



(d) Delay Line Output

FIGURE 2. SYSTEM WAVEFORMS AND CHARACTERISTICS

The envelope of the output of the delay line is shown in Figure 2(d). It is a $\sin x/x$ waveform with a pulse width very near $1/B_c$ and delayed by T_b seconds from zero time, where T_b is the delay corresponding to the (low) frequency $(f_1 + f_0)$ applied to the delay line at zero time.

If the input frequency is shifted from f_0 , the center of the chirp spectrum at the delay line input will be correspondingly shifted. Due to the linear delay versus frequency characteristic of the line, the compressed output will be proportionately shifted in time. Define a to be the slope of the frequency versus delay characteristic of the delay line. Since the delay line is matched to the input chirp a is equal to B_c divided by T_c .

$$a = \frac{B_c}{T_c} \text{ sec}^{-2} \quad (1)$$

Thus for a shift of f Hz in the input spectrum, the output pulse is shifted by τ seconds, where

$$\tau = \frac{f}{a} \quad (2)$$

The frequency resolution (bandwidth) Δf of the system is equal to the frequency required to shift the output pulse by its width $1/B_c$. Letting $\tau = 1/B_c$, we have

$$\frac{1}{B_c} = \frac{\Delta f}{a} \quad (3)$$

$$\Delta f = a \frac{1}{B_c} = \frac{1}{T_c} \quad (4)$$

Hence the frequency resolution of the system is equal to the reciprocal of the chirp duration. To realize a 100 kHz resolution a 10 μ s chirp pulse is required.

The time bandwidth product of the dispersive delay line must be greater than that of the input chirp to accommodate the input spectrum. Assume that f_0 is the center frequency of the input spectrum and that the spectrum to be

analyzed is contained in the band between $f_o - \frac{B_i}{2}$ to $f_o + \frac{B_i}{2}$, so that B_i is the width of the band to be analyzed. The dispersive delay line must have a linear delay from $(f_1 + f_o - \frac{B_i}{2})$ to $(f_2 + f_o + \frac{B_i}{2})$, which is a bandwidth of $B_c + B_i$. The variation in delay T_d of the delay line over this band is given by

$$T_d = \frac{B_i + B_c}{a} \quad (5)$$

so that the time-bandwidth product of the delay line is

$$T_d (B_i + B_c) = \frac{(B_i + B_c)^2}{B_c} T_c \quad (6)$$

The bandwidth of the input chirp B_c is a free parameter. It proves convenient to chose it so as to minimize the time-bandwidth product of the delay line.

This is accomplished by choosing B_c equal to B_i . In this case

$$T_d (B_i + B_c) = 4 T_c B_c = 4 T_c B_i \quad (7)$$

The time-bandwidth product of the delay line is therefore four times the time-bandwidth product of the input chirp.

The number of filters N realized by this technique is the input bandwidth B_i divided by the frequency resolution Δf

$$N = \frac{B_i}{\Delta f} = B_i T_c \quad (8)$$

In the case where $B_c = B_i$, the number of filters is the time-bandwidth product of the chirp.

2. Design Example

Suppose that it is required to design a bank of filters with 125 kHz resolution to analyze a 5 MHz band. We have $B_i = 5 \text{ MHz}$ and $T_c = 1/125 \text{ kHz} = 8 \mu\text{s}$. Choosing B_c equal to B_i , the time bandwidth product of the chirp is $(8\mu\text{s})(5 \text{ MHz}) = 40$ and that of the delay line is $4(40) = 160$. The delay line has total delay $T_d = 16 \mu\text{s}$ and bandwidth 10 MHz.

Table 1. Summary of Design Example

Input Bandwidth	B_i	5 MHz
Frequency Resolution	Δf	125 kHz
Chirp Duration	T_c ($= 1/\Delta f$)	8 μ s
Chirp Bandwidth	B_c ($= B_i$)	5 MHz
Chirp Slope	$a = B_c/T_c$	$.625 \times 10^{12} \text{ s}^{-2}$
Chirp Time-Bandwidth	$T_c B_c$	40
Delay Line Bandwidth	$B_i + B_c$	10 MHz
Delay Line Differential Delay	T_d ($= \frac{B_i + B_c}{a}$)	16 μ s
Delay Line Time Bandwidth	$T_d (B_i + B_c)$	160

3. Prefiltering and Analysis Efficiency

The technique as hitherto described has two drawbacks. These are that the spectral analysis is not continuous but interrupted in time and that the response function has a $\sin x/x$ shape which has relatively poor sidelobes. Both these drawbacks can be eliminated. A method for achieving a more continuous analysis is described in this section and a method for improving the sidelobes is described in the next section.

Figure 3 depicts a chirp input to the delay line occurring in the interval zero to T_c . For convenience it is assumed that the delay line has zero delay at the maximum frequency to be processed, that is, $f_o + f_2 \neq B_i/2$, so that the output to an input sine wave at $f_o + B_i/2$ occurs at time T_c . When the input frequency is $f_o - B_i/2$, the output occurs at time $2T_c$, for the condition $B_c = B_i$.* (Figure 3(b) and 3(c).)

The delay line amplitude characteristic is assumed to be flat over the band $(B_i + B_c)$ from $(f_o + f_1 - B_i/2)$ to $(f_o + f_2 + B_i/2)$ and to fall off very steeply outside this band. If the input frequency exceeds $f_o + B_i/2$, a portion of the chirp pulse will be filtered out by the delay line, but the remainder will tend to compress. As shown on line (e) of Figure 3, the output pulse occurs at time $0.5 T$ for an input at $f_o + \frac{3B_i}{4}$. It has half the energy and twice the width compared with an output pulse due to a sine wave in the band from $(f_o - B_i/2)$ to $(f_o + B_i/2)$, therefore it is half amplitude.

Line (d) shows the output due to an input frequency below the bottom edge of the input band. For an input frequency of $f_o - \frac{3B_i}{4}$, the pulse occurs at $2.5 T$ and is half amplitude and double width.

* The spectral analysis is backward, i.e., high frequencies are on the left, however, this is easily corrected by reversing the direction of the chirp.

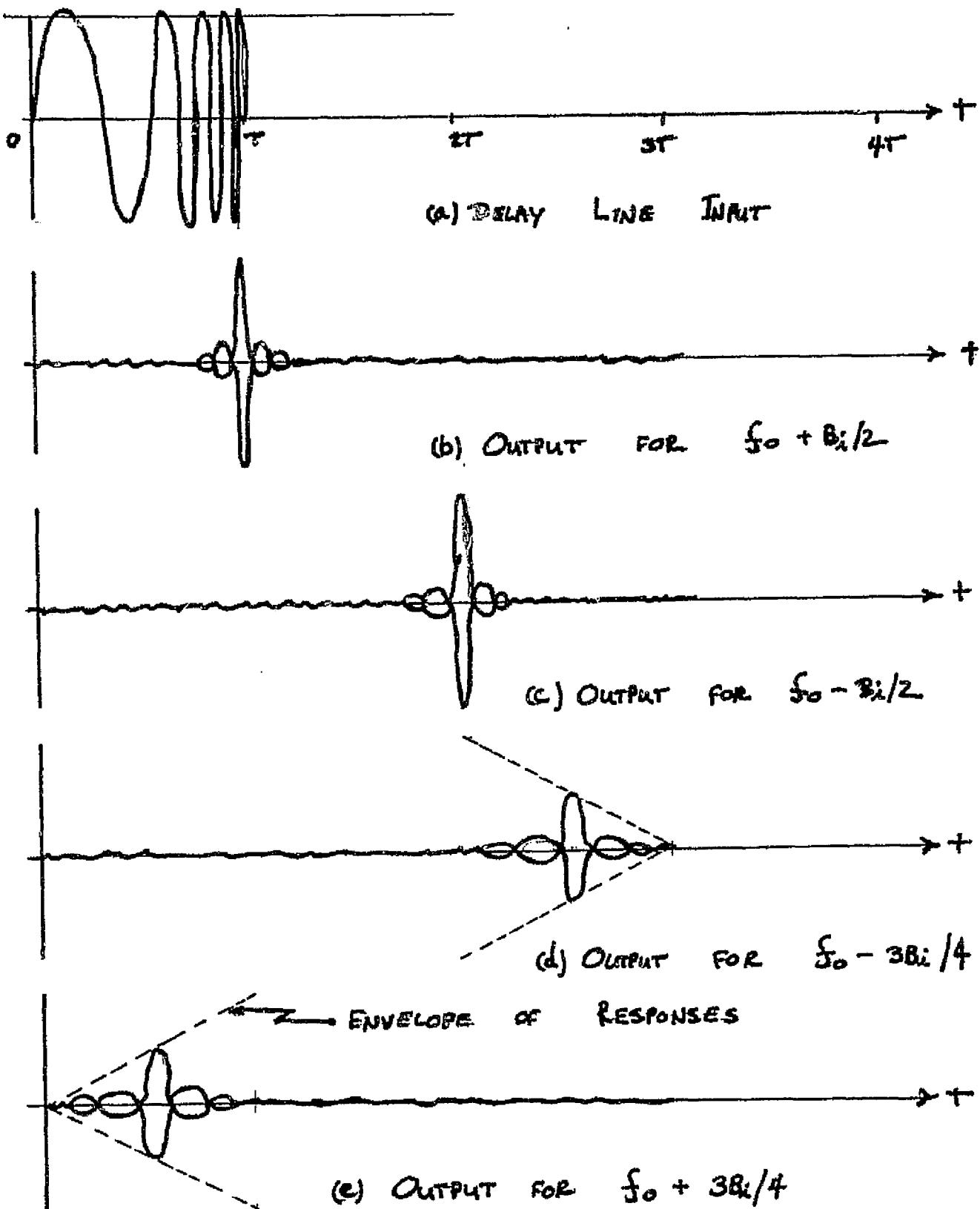


FIGURE 3. OUTPUTS AS A FUNCTION OF
INPUT FREQUENCY

In summary, an input to the delay line over the interval zero to T produces outputs over the period from 0 to $3T$. The outputs from 0 to T and from $2T$ to $3T$ are due to frequencies not in the input band B_i that is to be analyzed. The desired output occupies the interval from T to $2T$. Although the undesired outputs may be gated out, to avoid ambiguities, the delay line cannot be pulsed again until the interval from $3T$ to $4T$, and this reflects a $1/3$ duty ratio of the analysis.

The best method to alleviate this problem is to employ a prefilter prior to the filter bank that passes the band from $f_o - B_i/2$ to $f_o + B_i/2$ and rejects energy outside this band. If the prefilter were perfect, the analysis duty ratio would become one. Some tolerance must be allowed at the band edges, however, but use of a surface wave delay line filter with its steep edges would permit high analysis efficiency.

A second method is to make the chirp bandwidth B_c greater than the analysis band B_i . The effect of this is to compress the output spectral analysis in time, but it does not affect the frequency resolution. Using a combination of this method and prefiltering, it is possible to obtain 100% analysis efficiency.

4. Filter Shape

The shape of the output waveform is $\sin x/x$. The drawback to this response is to relatively high time sidelobes.

Sidelobe reduction is normally accomplished in pulse compression systems by performing weighting in the frequency domain. This is not possible in this technique because the chirp spectrum shifts with the input frequency. In this technique, however, the time of occurrence of the input chirp is known, (which is not generally the case in radar and communication applications) so that the weighting can be applied in the time domain. An amplitude modulator is placed in front of the input mixer and a weight function is generated in synchronism with the chirp pulse.

A computer run was performed to check this technique*. Hamming amplitude weighting was employed. The results are shown in Figure 4, for a time bandwidth product of 256. The input frequency is at the center of the band, so that the output pulse occurs in the middle of the interval. The response is excellent with -45 dB first sidelobes and most sidelobes below -50 dB.

5. Summary

A block diagram of the refined technique is shown in Figure 5. This is equivalent to Figure 1 with the addition of the input bandpass filter and the amplitude modulator to weight the chirp. The specific advantages of this technique are summarized below.

1. A filter bank is realized without the plethora of components that are usually necessary.
2. The difficulties of alignment are avoided by this technique. All filters will have the same resolution and gain to the extent the delay-frequency characteristic of the dispersive delay line is linear and to the extent the amplitude characteristic of the delay line is flat.
3. The filter shape is determined by the time domain weighting. Filter responses can be obtained that would require very elaborate (high order) combinations of inductors and capacitors.
4. Large filter banks require distribution amplifiers at their input to drive all the inputs and some sort of multiplexer to scan the outputs. The delay line technique has a single input and a single output.
5. A surface wave delay line is an ideal component for realizing both the input filter and the dispersive delay line. The only drawback to this component is that it is limited in delay to 20 μ s or so, thereby limiting the frequency resolution to 100 kHz or so. Use of this component gives a compact implementation, low power dissipation, and low cost.

* This work was performed by H. L. Groginsky and C. Shaw.

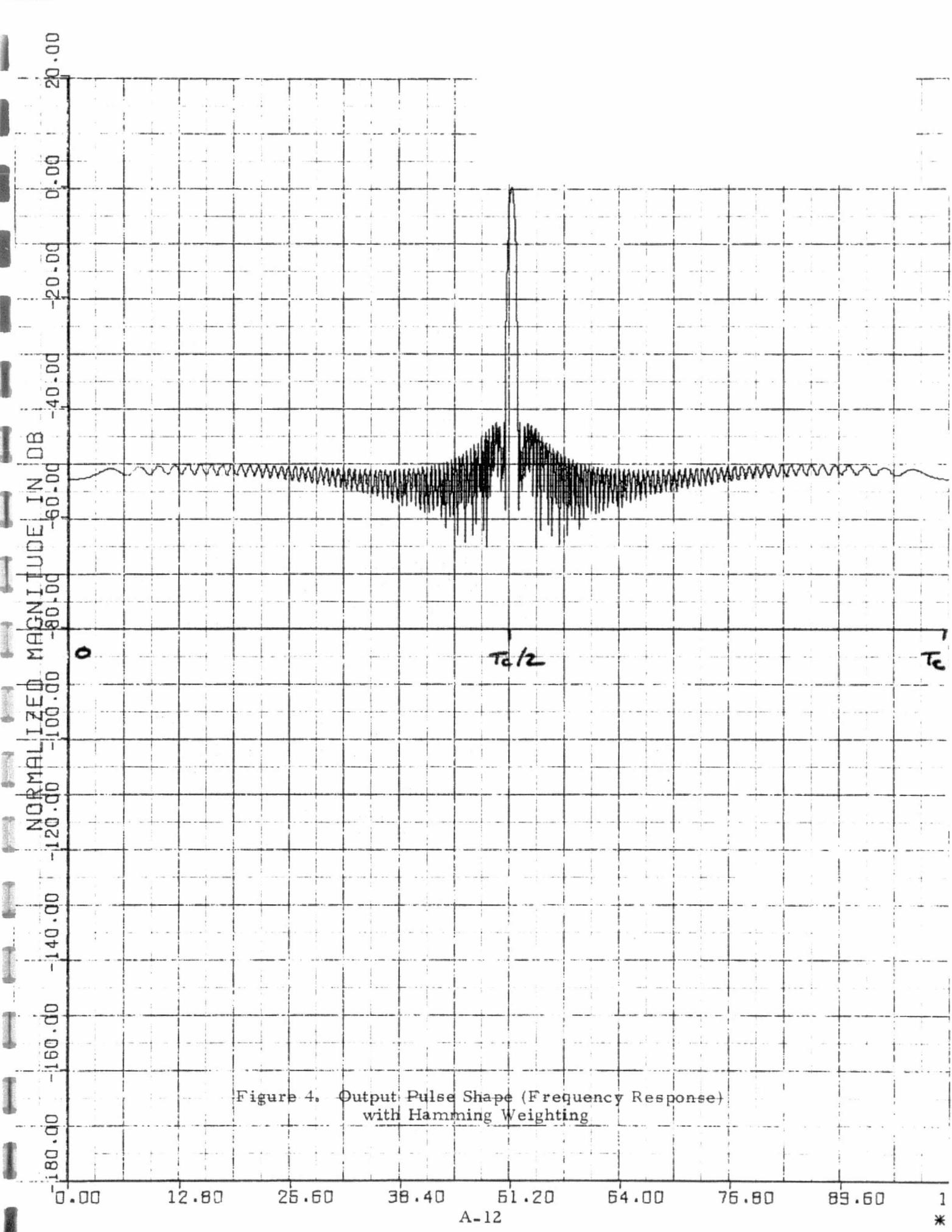


Figure 4. Output Pulse Shape (Frequency Response)
with Hamming Weighting

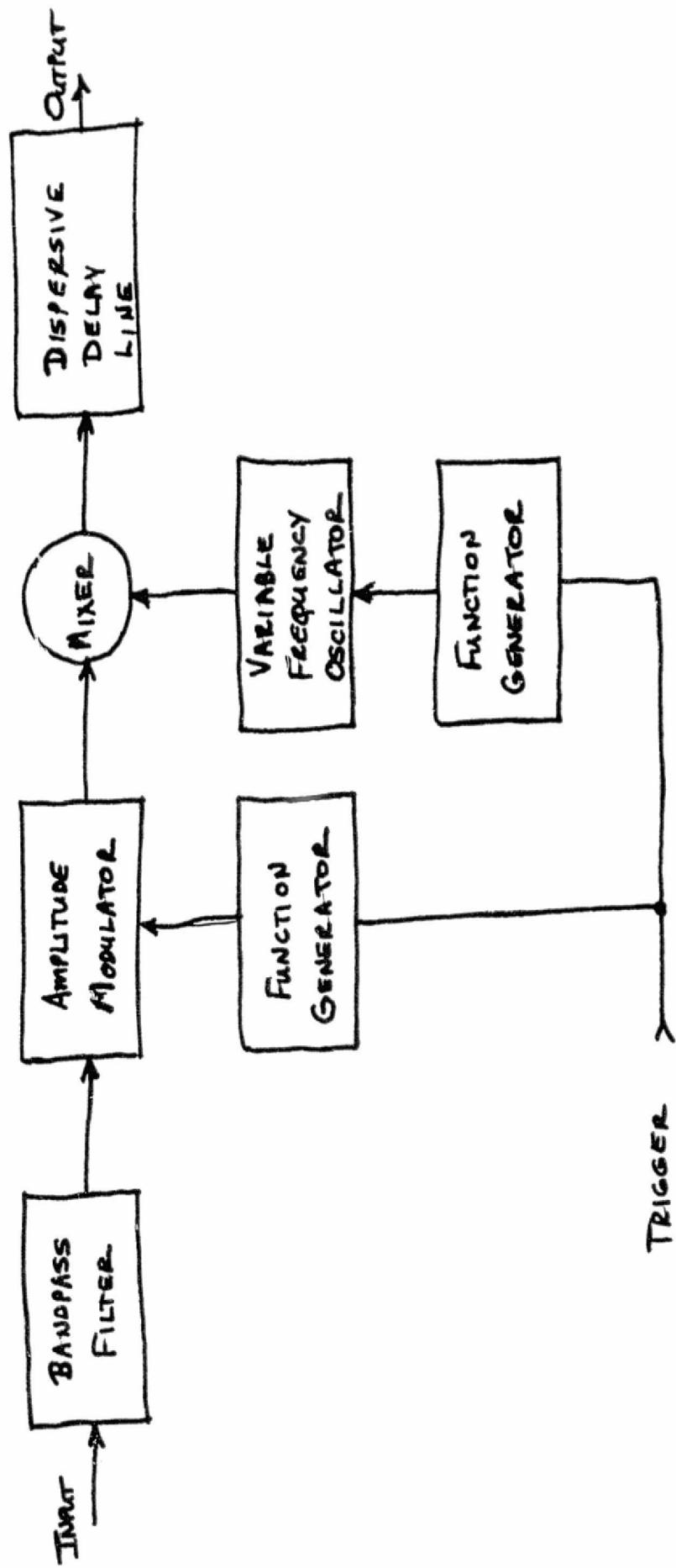


Figure 5. REFINED DESIGN

APPENDIX B

PbSnTe DETECTOR TESTS

A total of seven detector chips in two dewars (made by North American Rockwell) were tested. These PbSnTe detector chips are about 230μ square and the chips are cooled with liquid nitrogen.

The detectors were tested using two off-set lasers. In addition, an x-y recorder was used to generate the I-V-P curves shown in Figures 1 through 7. From the I-V-P curves, one can determine the static and dynamic responsivity, quantum efficiency and resistance; additionally, saturation and voltage breakdown can be determined.

By measuring the S/N under different bias conditions, the optimum operating point for each detector chip was determined from Figures 8 to 14. Since some chips produced what appeared to be $1/f$ noise (see Figure 15) the S/N was a function of frequency. For this reason the S/N was measured as a function of frequency as shown in Figure 16.

Next, frequency response curves were obtained from the heterodyne signal of two offset lasers as shown in Figure 17. When the shot noise spectrum was compared to the heterodyne signal response, a discrepancy was noticed. Also, theoretical calculations of the frequency response from capacitance measurements produced still different results.

The results of further investigation of this effect by Raytheon showed that the frequency response depended upon the exact position of the focussed spot on the detector chip. This means that large changes in system response at frequencies beyond 5 mHz can occur with slight shifts in detector position. The manufacturer said he had not observed this problem and the $1/f$ noise problem before and said he would replace the chips with new ones.

A complete summary of the test results is given in Figure 18. Chips #1 in both dewars seemed to be the best, having 35% to 45% dynamic quantum efficiencies and being within 2 or 3 dB of being shot noise limited. The early saturation at about 2 mw prevented reaching the shot noise limit.

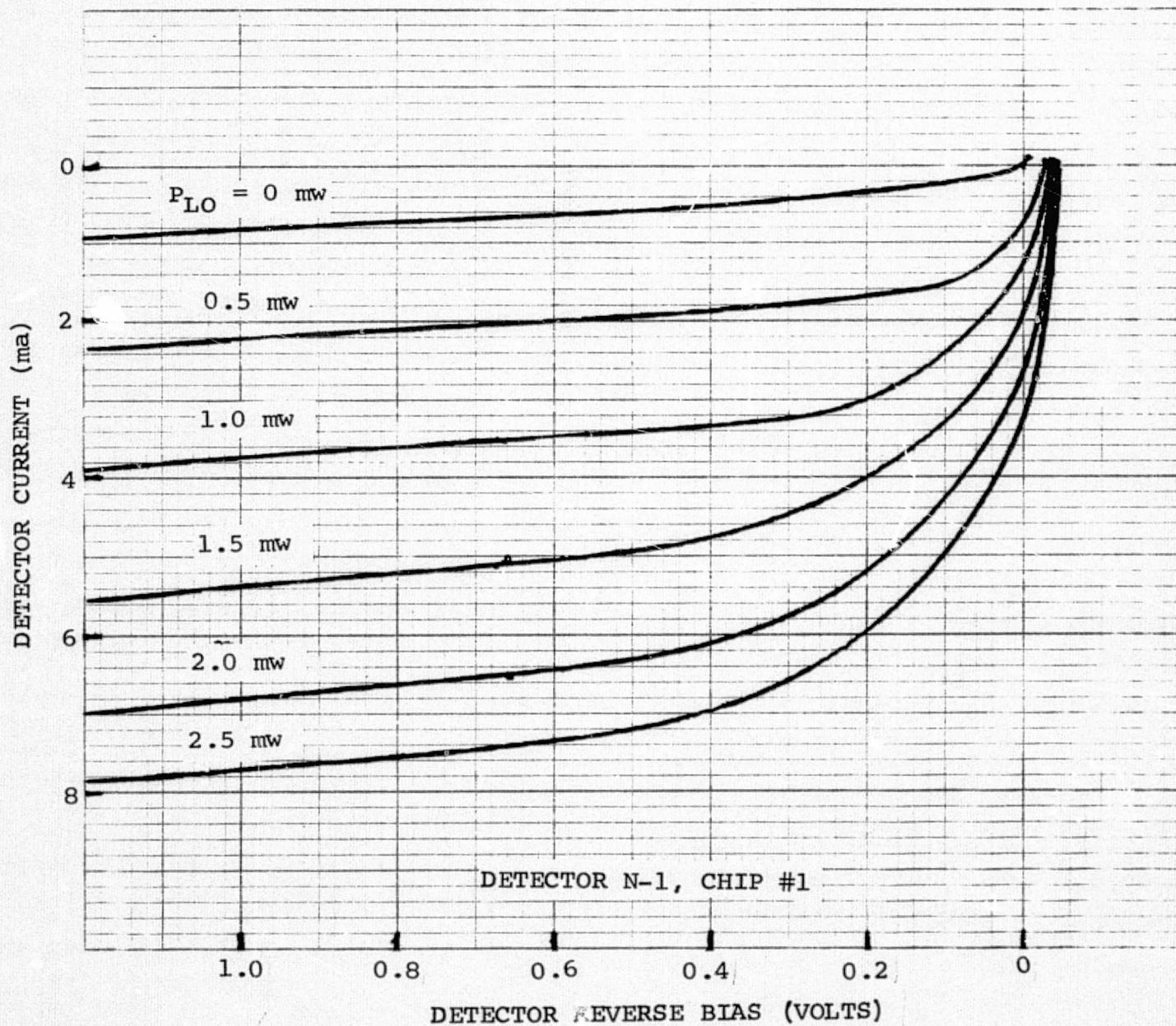


Figure 1. I-V-P Curves, Detector N-1, Chip No. 1

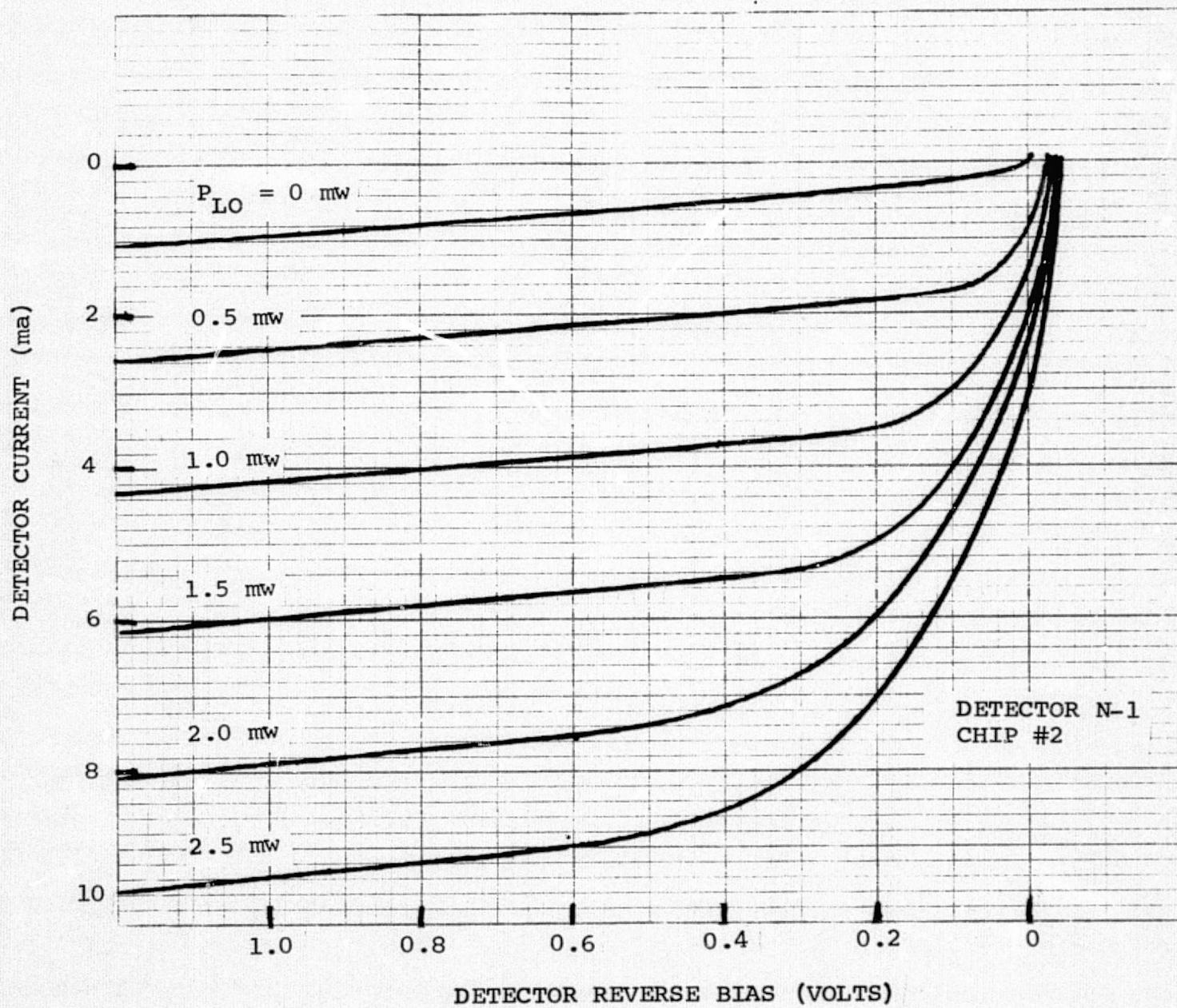


Figure 2. I-V-P Curves, Detector N-1, Chip No. 2

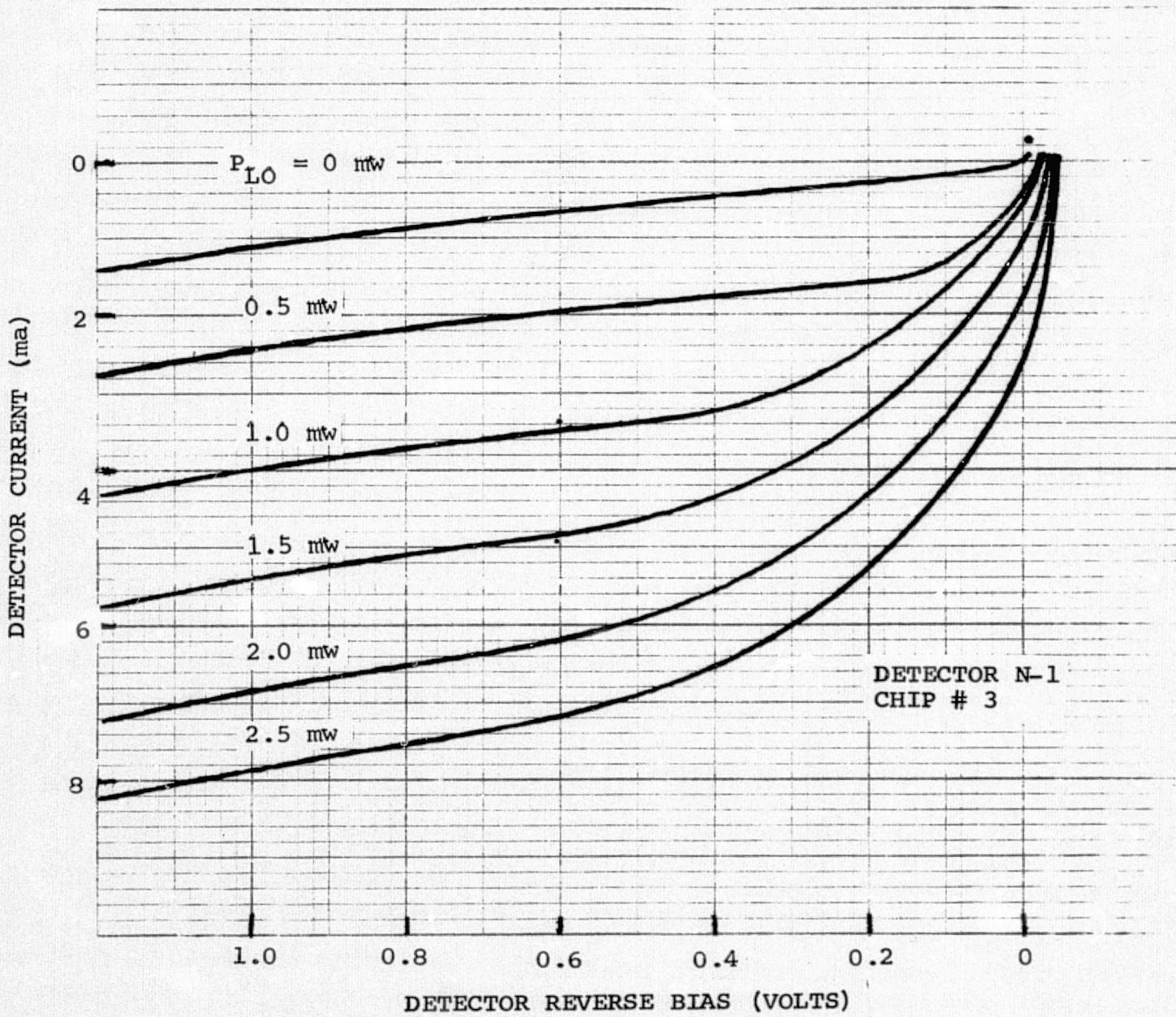


Figure 3. I-V-P Curves, Detector N-1, Chip No. 3

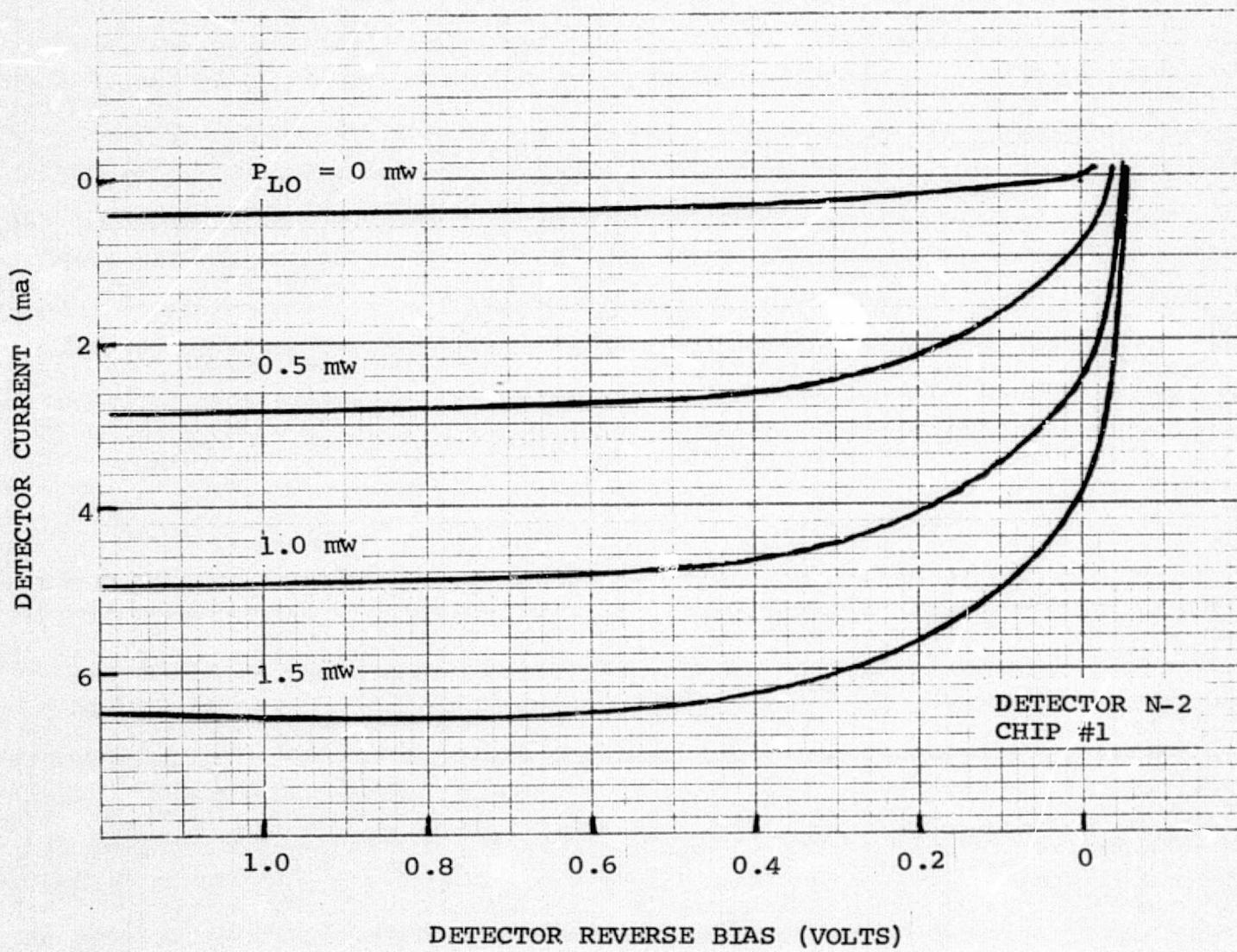


Figure 4. I-V-P Curves, Detector N-2, Chip No. 1

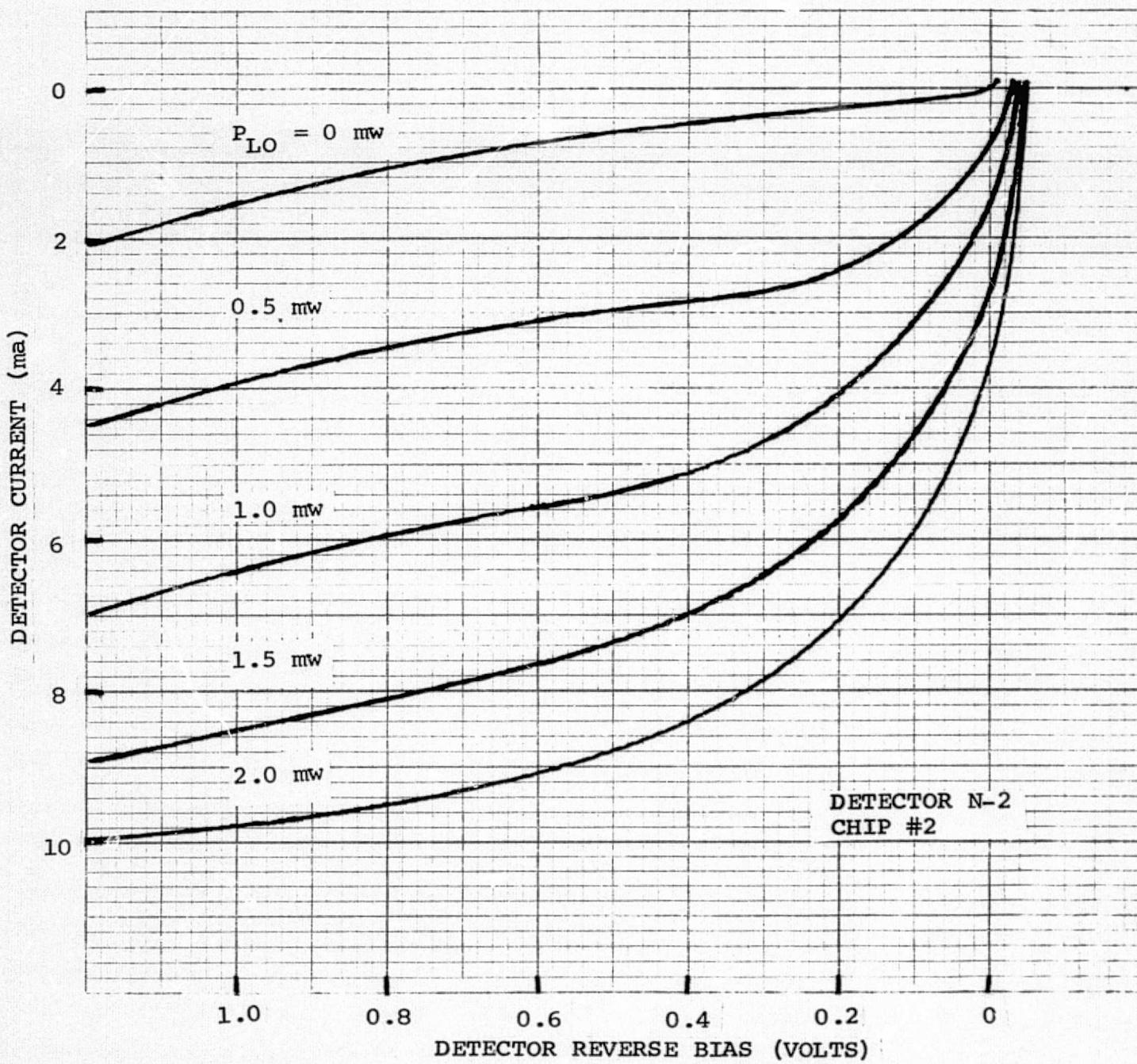


Figure 5. I-V-P Curves, Detector N-2, Chip No. 2

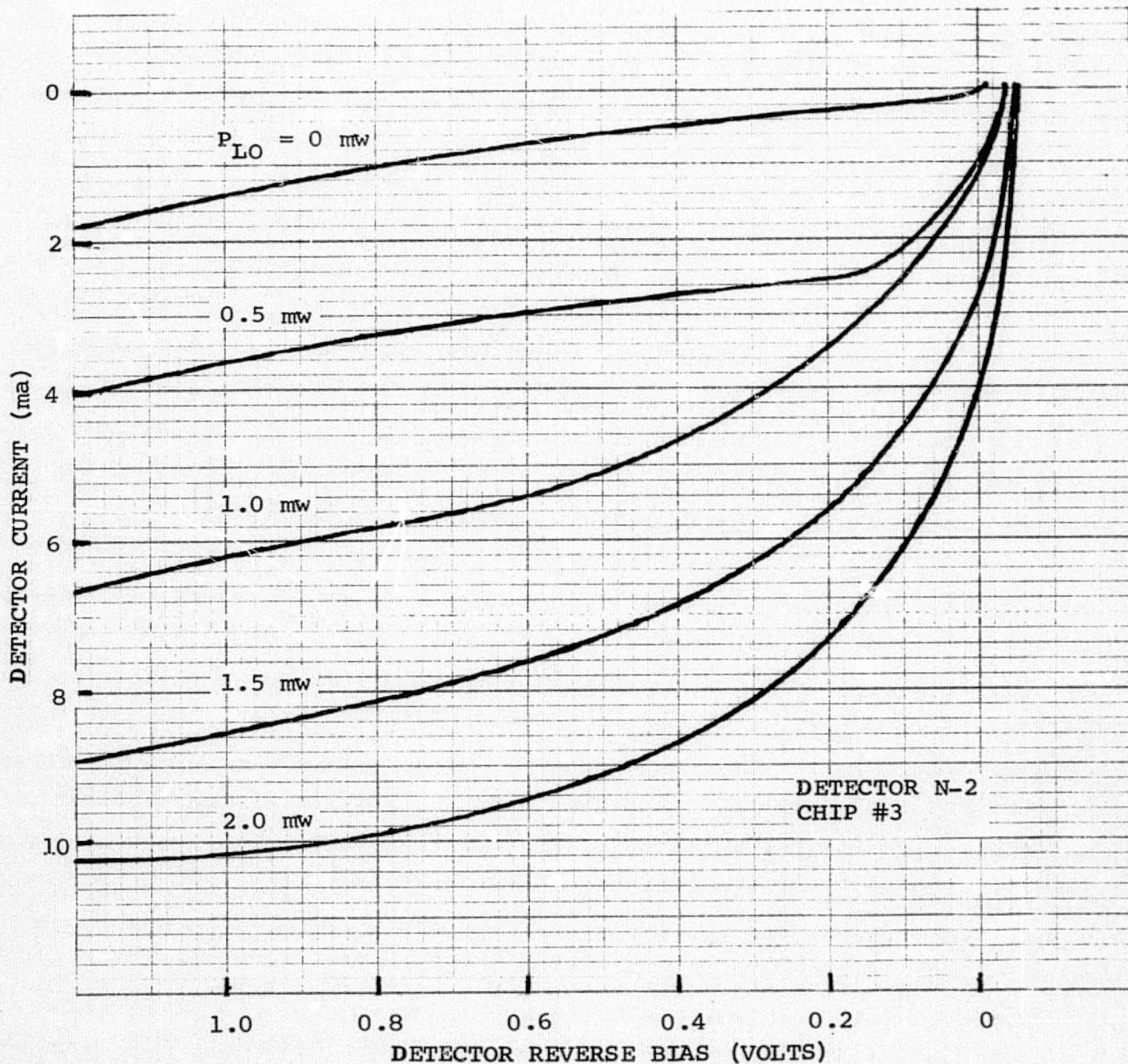


Figure 6. I-V-P Curves, Detector N-2, Chip No. 3

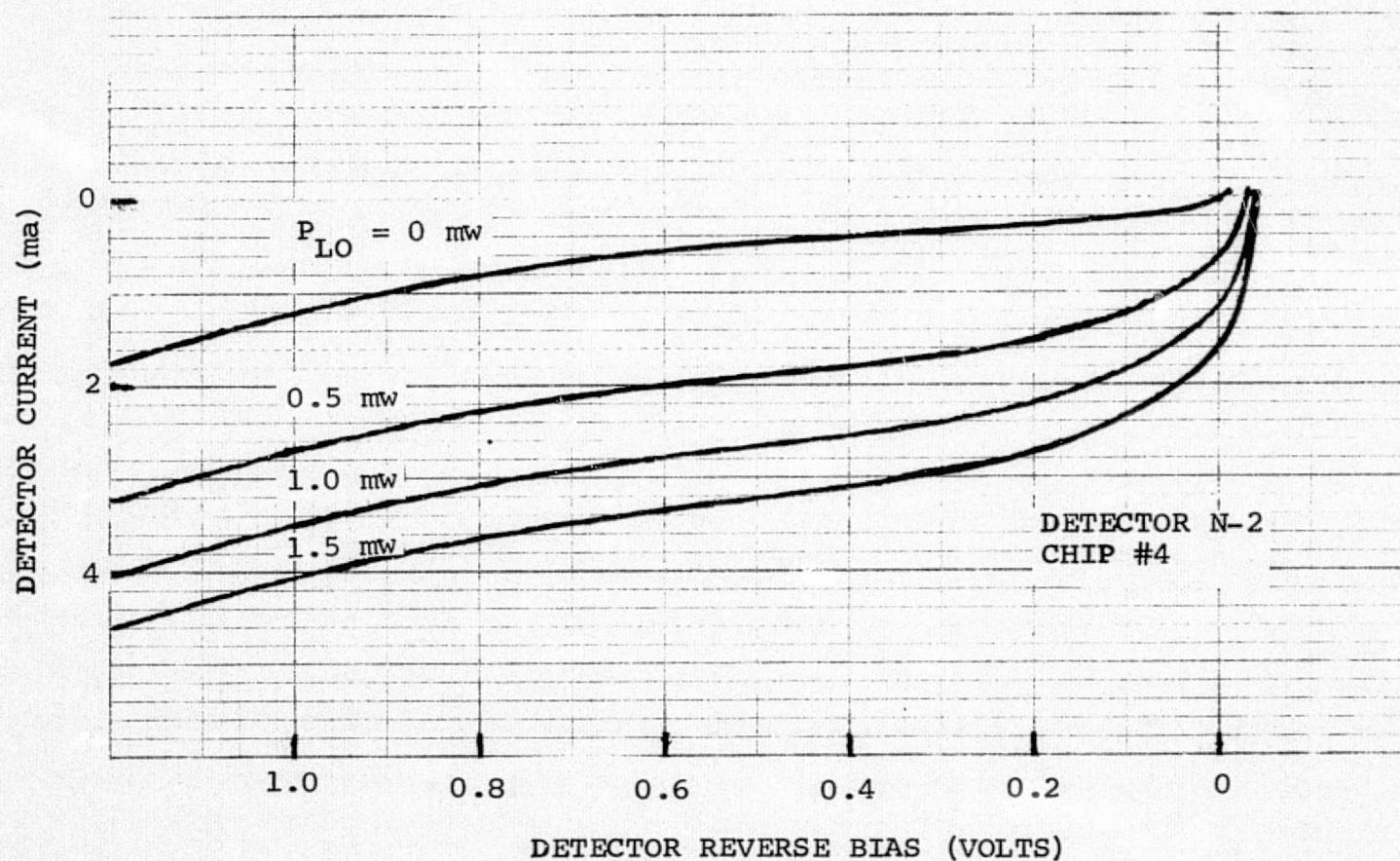


Figure 7. I-V-P Curves, Detector N-2, Chip No. 4

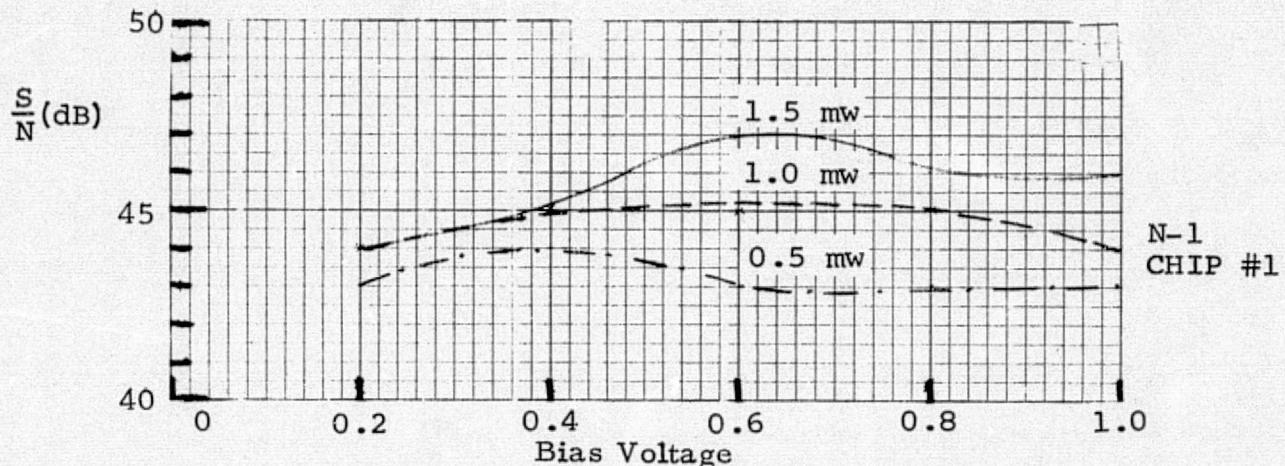


Figure 8. Bias Optimization Curves, Detector N-1, Chip No. 1

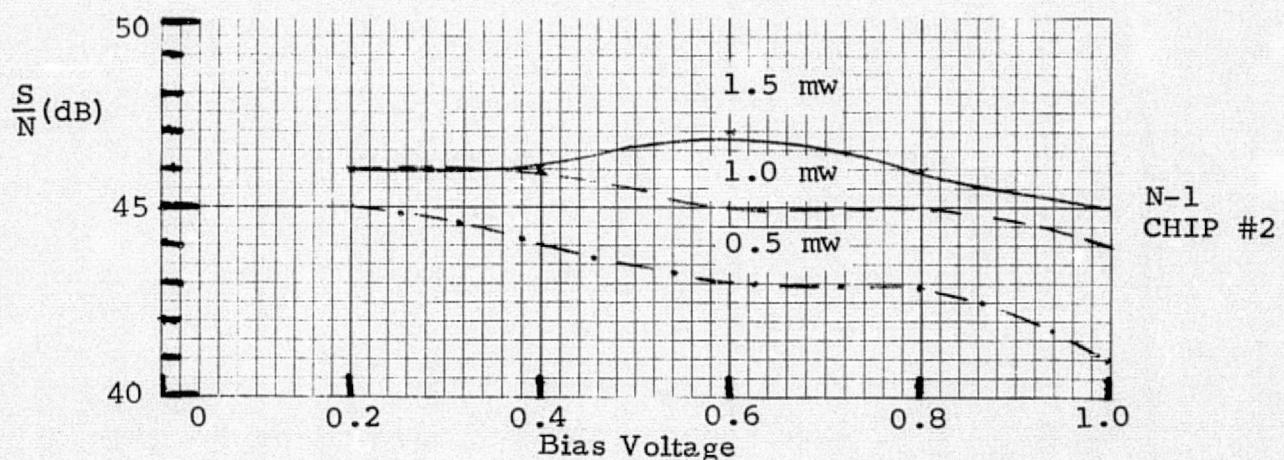


Figure 9. Bias Optimization Curves, Detector N-1, Chip No. 2

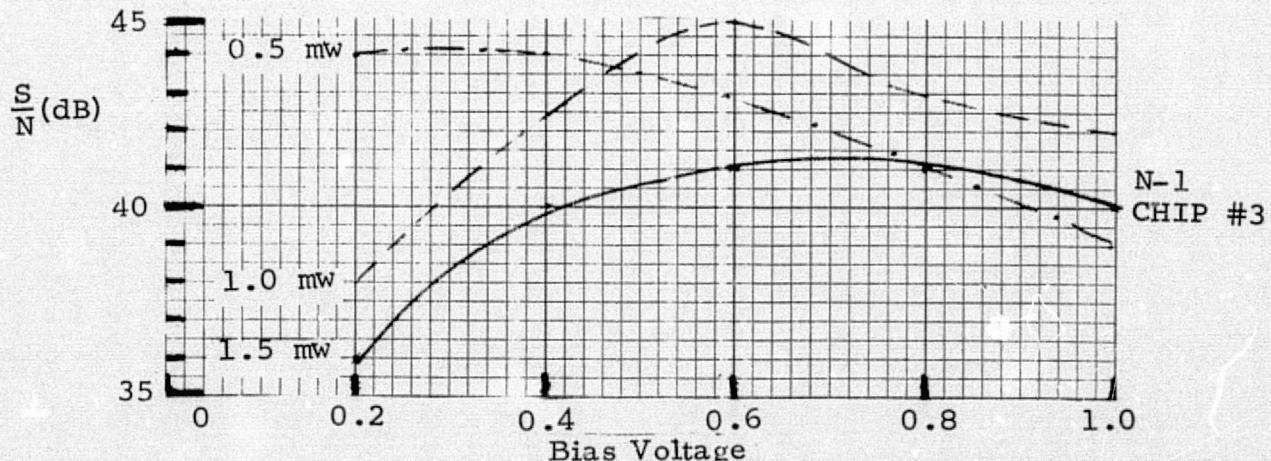


Figure 10. Bias Optimization Curves, Detector N-1, Chip No. 3

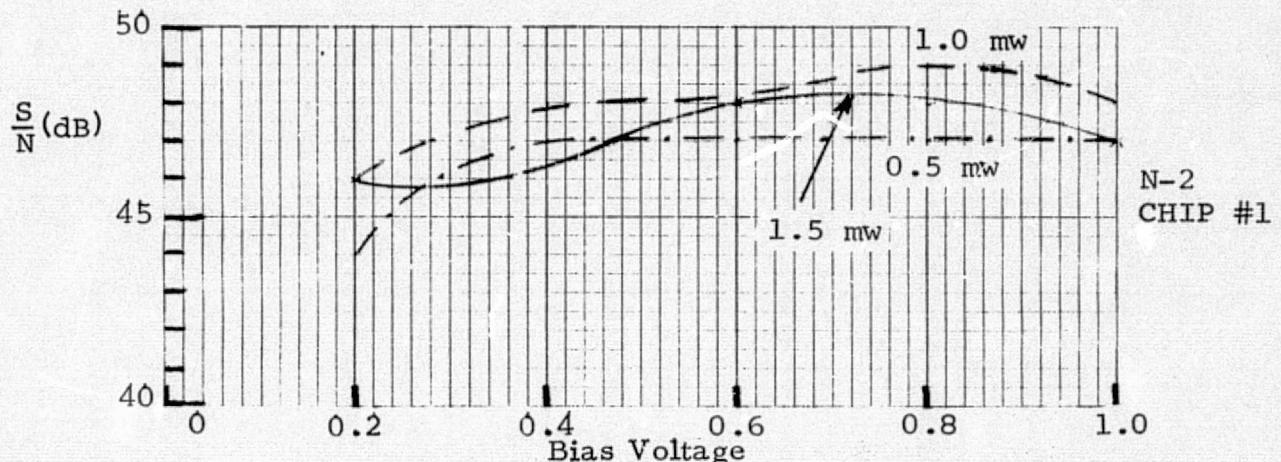


Figure 11. Bias Optimization Curves, Detector N-2, Chip No. 1

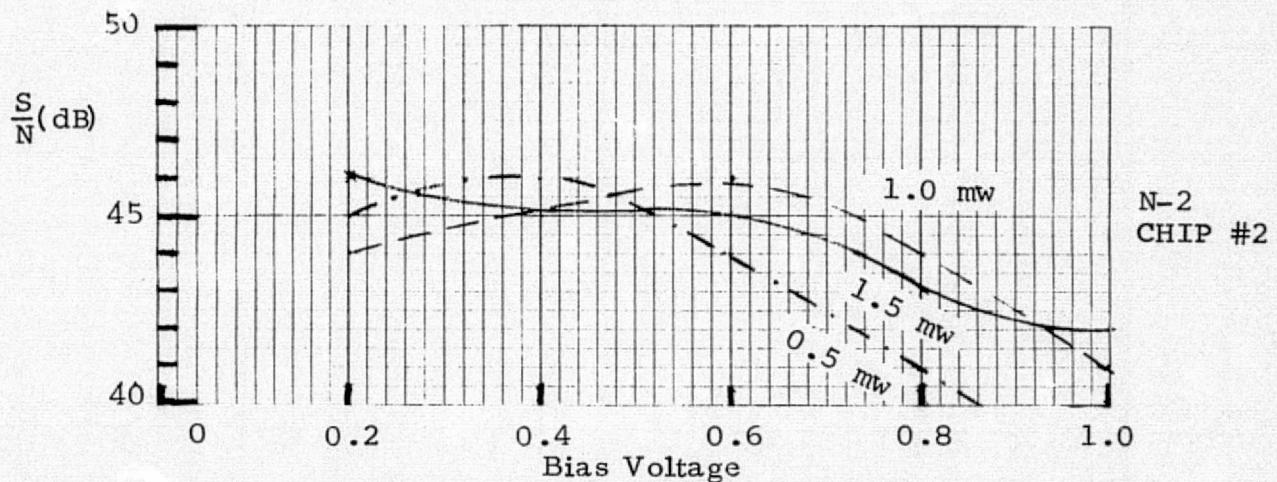


Figure 12. Bias Optimization Curves, Detector N-2, Chip No. 2

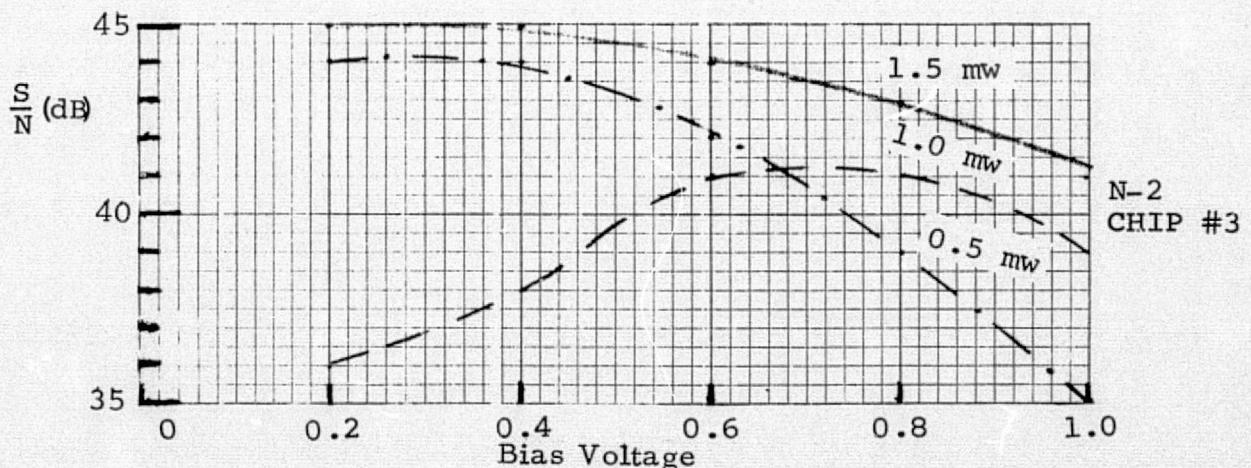


Figure 13. Bias Optimization Curves, Detector N-2, Chip No. 3

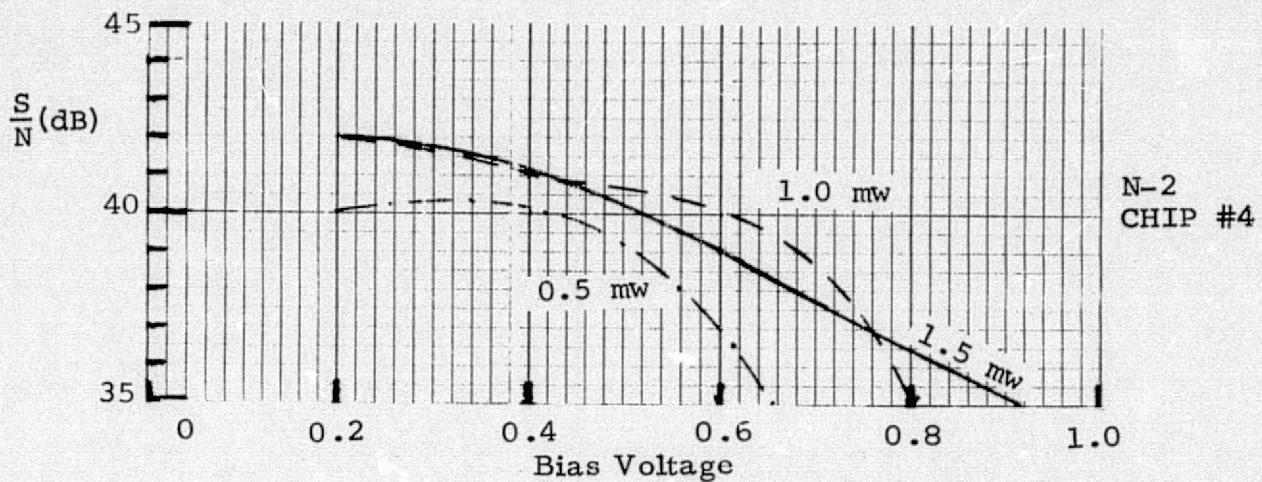
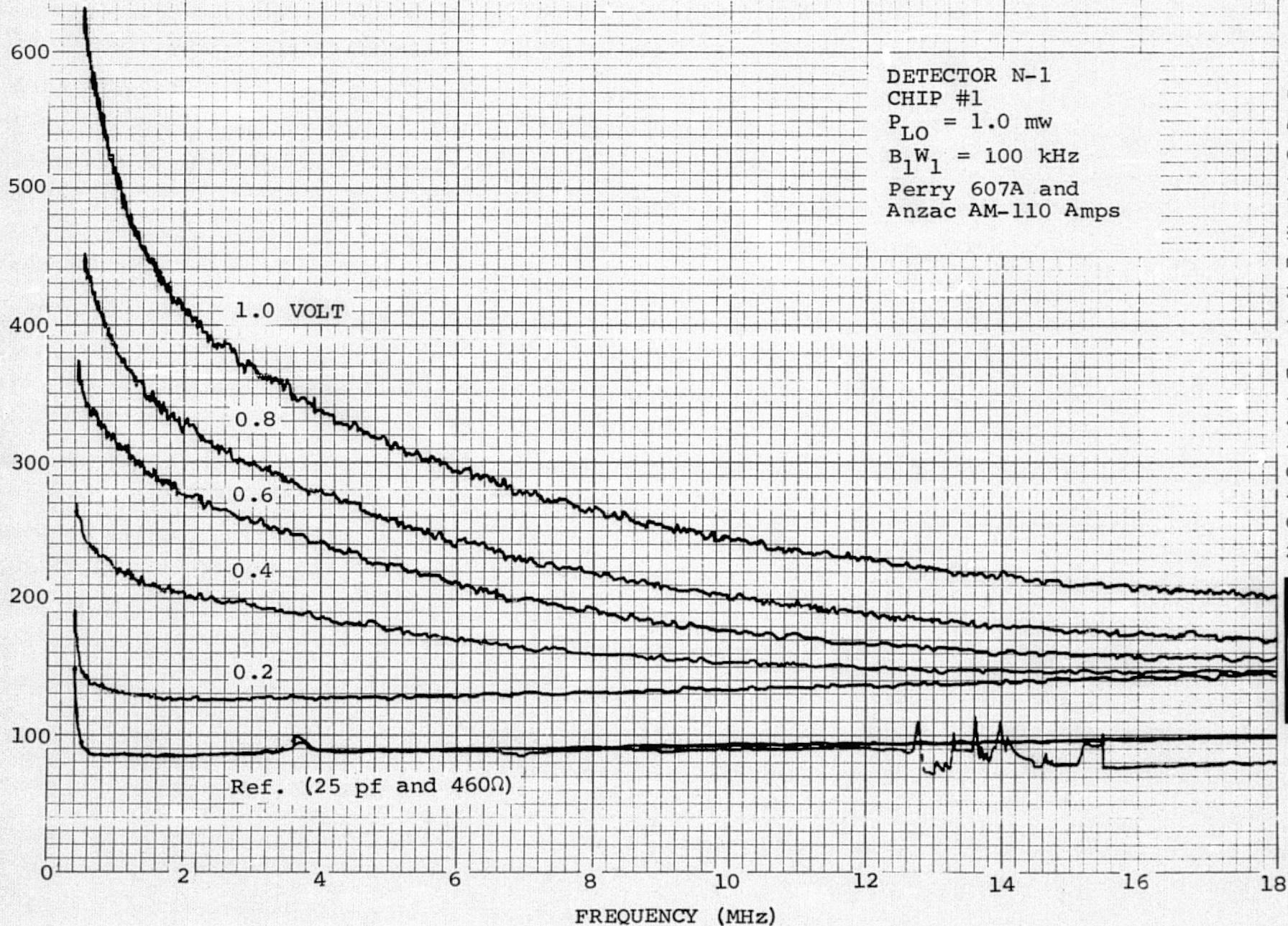


Figure 14. Bias Optimization Curves, Detector N-2, Chip No. 4

Figure 15. $\frac{1}{f}$ Noise vs. Bias Voltage



BW = 100 kHz

P_{LO} = 1 mW

V_D = 0.8 V

Old Vortex Receiver and
New Vias Circuit

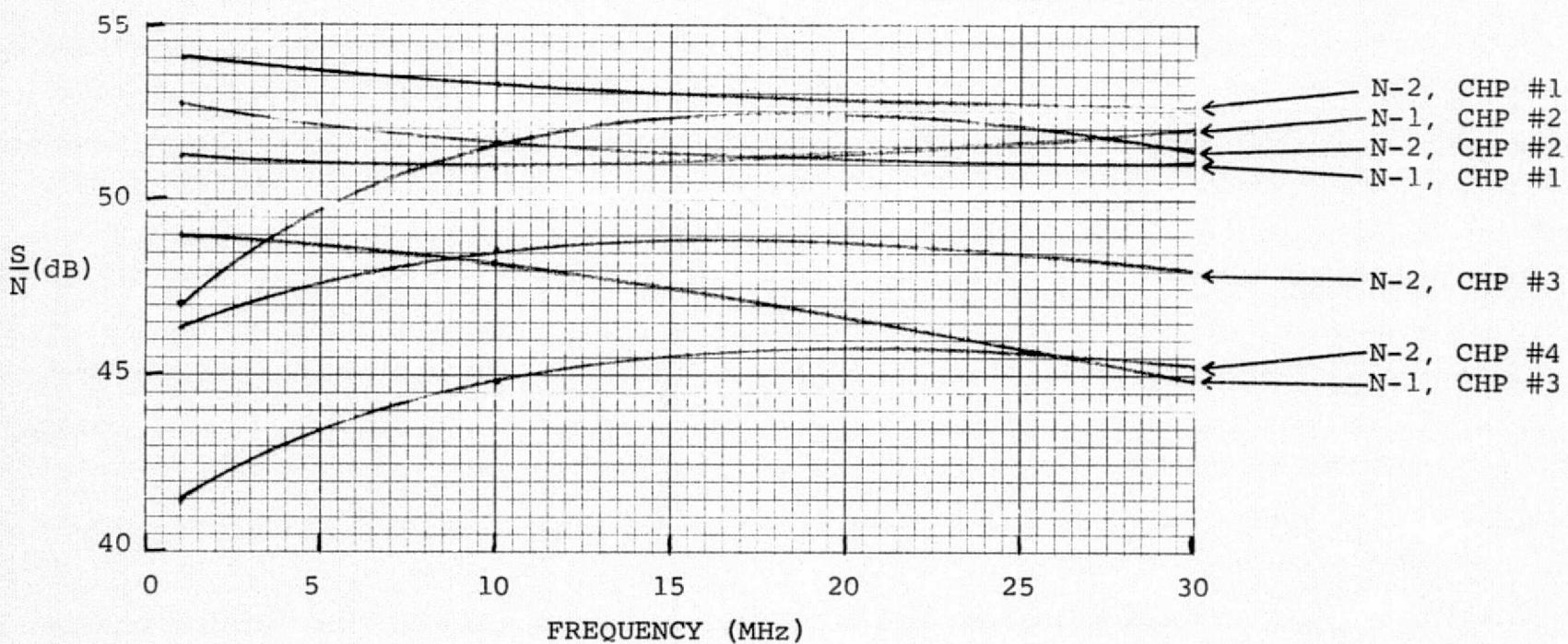


Figure 16. S/N vs. Frequency

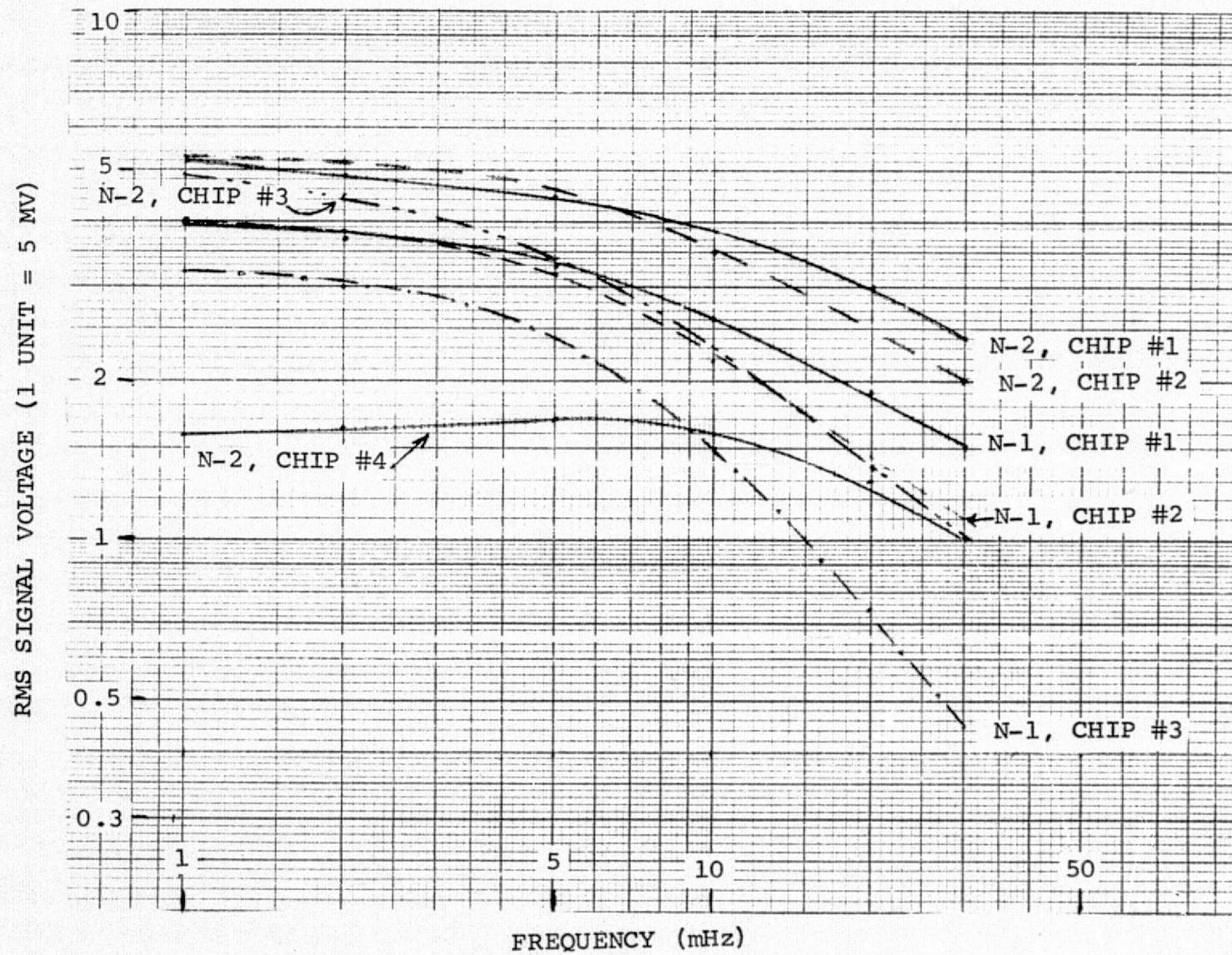


Figure 17. Heterodyne Signal Voltage vs. Frequency

RAYTHEON COMPANY
EQUIPMENT DIVISION



Parameters	Detector N-1			Detector N-2				Units
	Chip							
Dynamic Responsivity ⁽¹⁾	3.0	3.6	2.7	3.7	4.5	4.3	1.3	A/W
Dynamic Quantum Efficiency ⁽¹⁾	35	42	33	44	52	49	14	%
Nearness to Shot(1 MHz) Noise Limited Operation (10 MHz)	1.8 2.0	2.0 1.7	8.0 4.2	2.8 3.3	5.1 4.0	5.1 5.3	5.8 3.1	dB
f_c (3 dB) ⁽²⁾	4.3	3.7	5.6	11.5	8.8	4.8	23	kHz
Dynamic Resistance	910	1000	800	3500	400	220	360	Ω
Static Resistance	125	113	176	170	118	60	69	Ω
λ Test	P-20	P-Line						
P_{LO} Sat.	2.5	2.5	2.5	1.5	2.0	2.0	1.5	mW
Optimum P_{LO} Bias V_d (1 MHz) I_d	1.5 0.6 4.8	1.5 0.6 5.3	1.0 0.6 3.4	1.0 0.8 4.7	1.0 0.6 5.1	1.5 0.4 6.7	1.0 0.2 2.9	mW V mA
Dewar Hold Time	> 8	Same	Same	> 8	Same	Same	Same	Hr.

Note (1) Dynamic response measured at optimum bias conditions.

Note (2) The frequency response, f_c , depends on chip position and focus spot size. (See text.)

Figure 18. Detector Summary